

SK1/MY5 BLOCK DIAGRAM

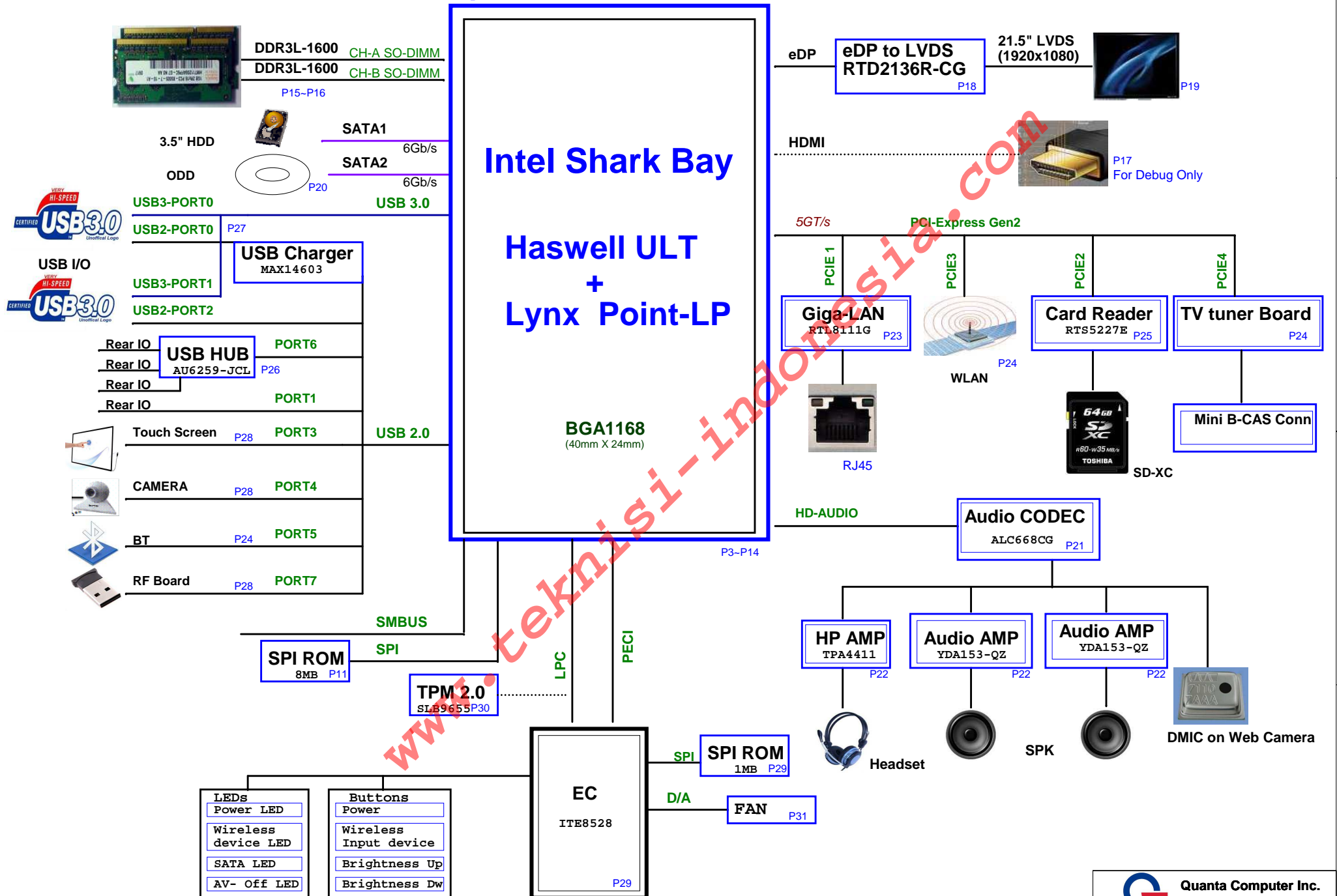


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Voltage Rails

Power	Voltage	S0	S3	S4	S5	Ctl Signal
+5VPCU	5V	V	V	V	V	5V_ALW
+3VPCU	3.3V	V	V	V	V	3V_ALW
5V_ALW	5V	V	V	V	V	+5VPCU_6686
3V_ALW	3.3V	V	V	V	V	+5VPCU_6686
3V_LAN	3.3V	V	Note	Note	Note	12V_LAN_ON
5V_S5	5V	V	V	V	V	12V_S5_ON
3V_S5	3.3V	V	V	V	V	12V_S5_ON
+1.35V_SUS	1.35V	V	V			S3_ON
+0.675V_DDR_VTT	0.675V	V	V			S3_ON
DDR_VTTREF	0.675V	V	V			S3_ON
+1.05V	1.05V	V				S0_ON_2
1.5V_S0	1.5V	V				S0_ON_1
12V_S5	12V	V	V			5V_S5
12V_S0	12V	V				12V_S0_ON1
5V_S3	5V	V	V			12V_S3_ON
3V_S3	3.3V	V	V			12V_S3_ON
5V_S0	5V	V				12V_S0_ON1
3V_S0	3.3V	V				12V_S0_ON1
+VCC_CORE	BY VID	V				VRON

Note : Deoend on WOL

F/W List

	Location	Update method
BIOS/ME	U5	Flash tool in Windows
EC	U38	Flash tool in Windows
LAN	U44	Flash tool in Windows
USB HUB	U45	Flash tool in Windows
Converter	U37	Flash tool in Windows

Resister tolerance:
F :+/- 1%, (example:69.8K/F_4)
others are +/- 5%, (example:69.8K_4)
Capacitor tolerance:
X7R: +/- 10%
X5R: +/- 10%
Y5V: +80%~-20%
others are +/- 5%

PCB STACK UP

6L

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

02



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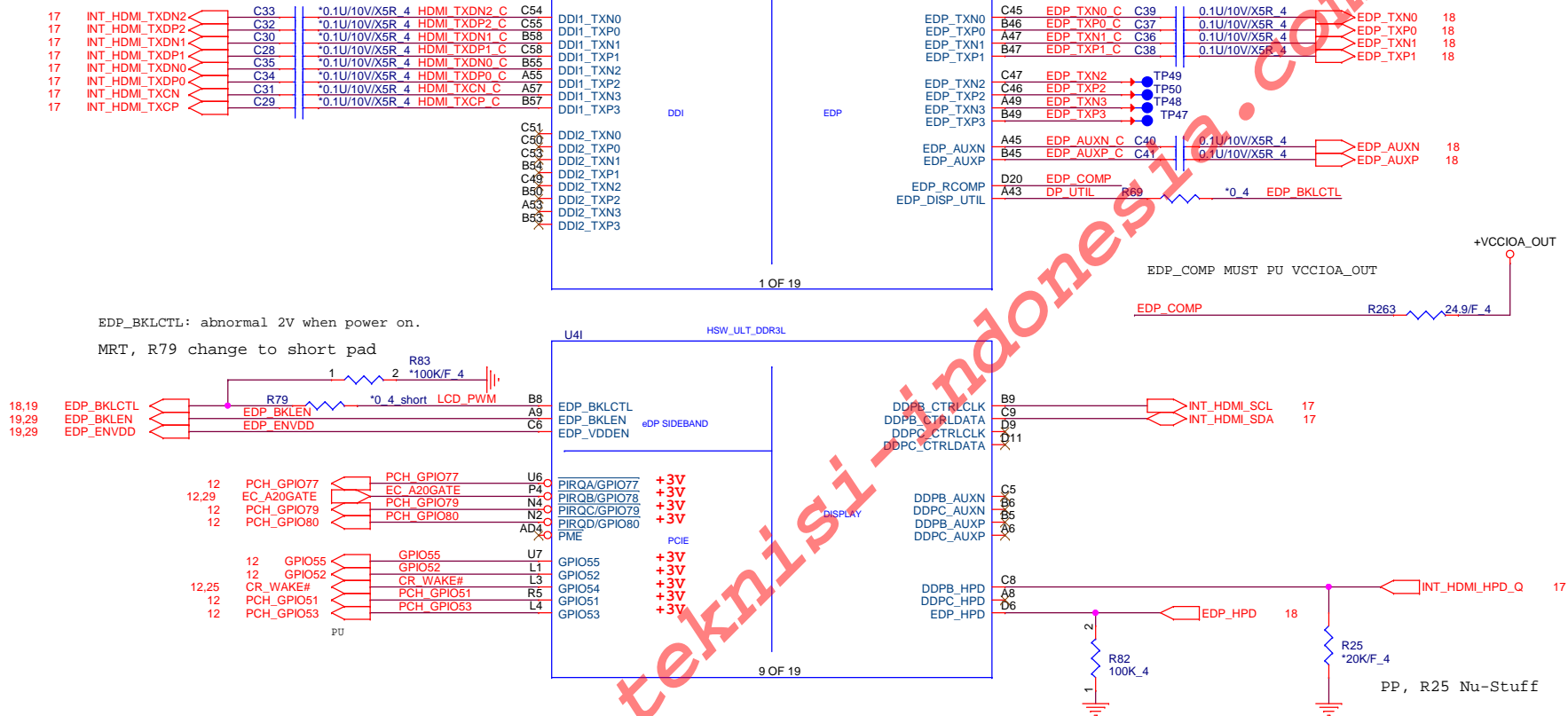
PROJECT : MY5

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Frontpage		
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Haswell ULT (DISPLAY)

PP, C33,C32,C30,C28,C35,C34,C31,C29 Nu-Stuff

HDMI For Debug



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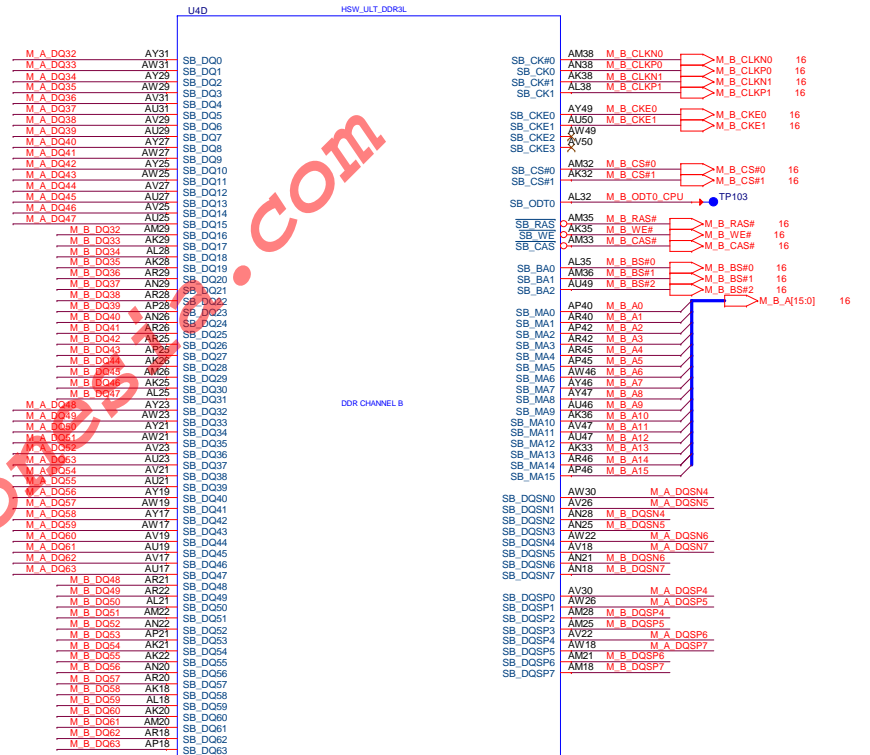
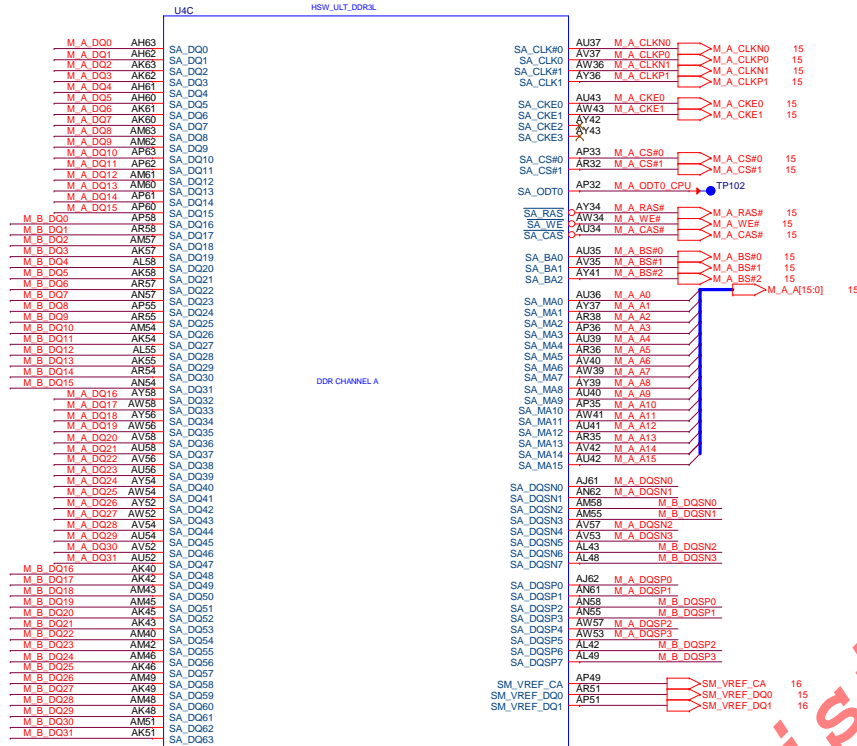
PROJECT : MY5

Size	Document Number	Rev
	HSW MCP(Display/eDP)	A

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Haswell ULT (DDR3L Interleaved PIN)

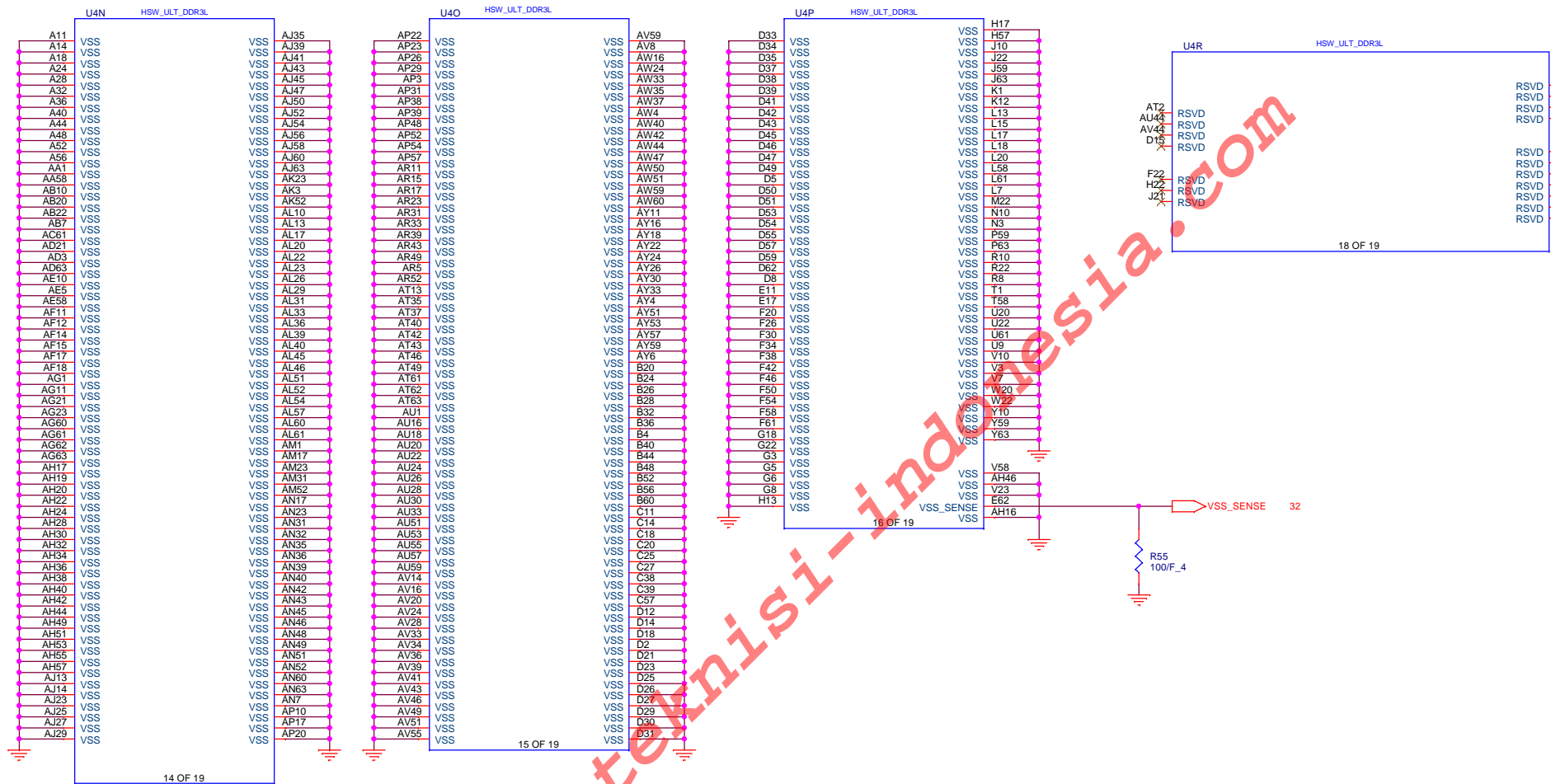
15 M_A_DQ[63:0] M_A_DQS[7:0] 15
 16 M_B_DQ[63:0] M_B_DQS[7:0] 16
 M_A_DQS[7:0] 16
 M_B_DQS[7:0] 16



1. Level 1 Environment-related Substances should Never be Used.
 2. Recycled Resin and Coated Wire should be procured from Green Partners.

Haswell ULT (GND)

05

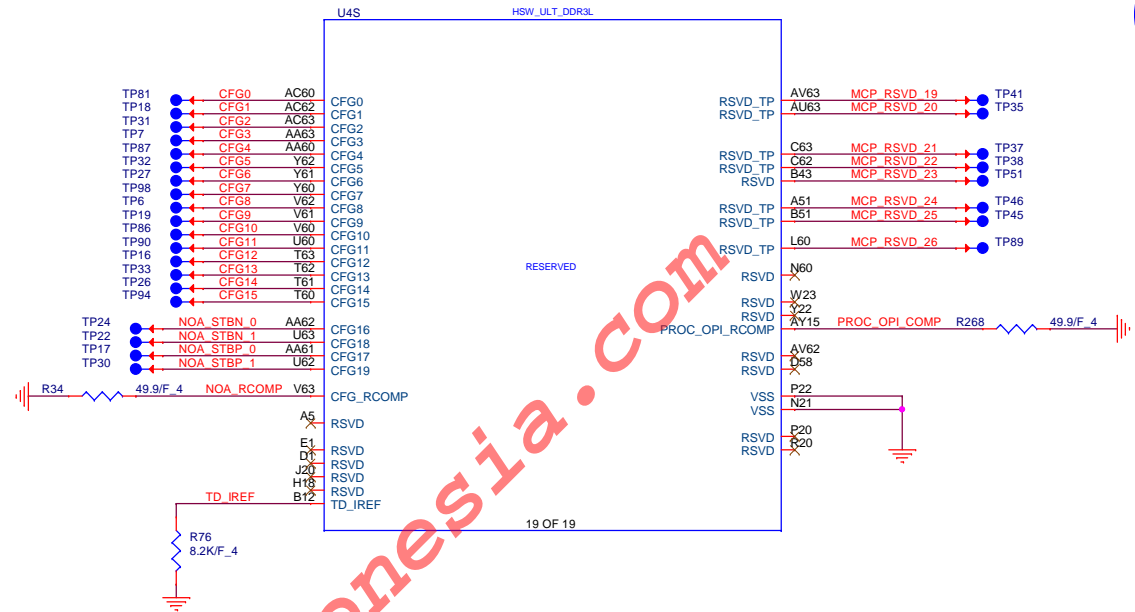


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PROJECT : MY5

Size	Document Number	Rev
	HSW MCP(GND/RSVD)	A
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Processor Strapping

	1	0	
CFG[2:0] Reserved configuration lane.			
CFG[3] MSR Privacy Bit Feature	(DEFAULT) Debug Capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting	IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden	
CFG[4] DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
CFG[19:5] Reserved configuration lanes.			

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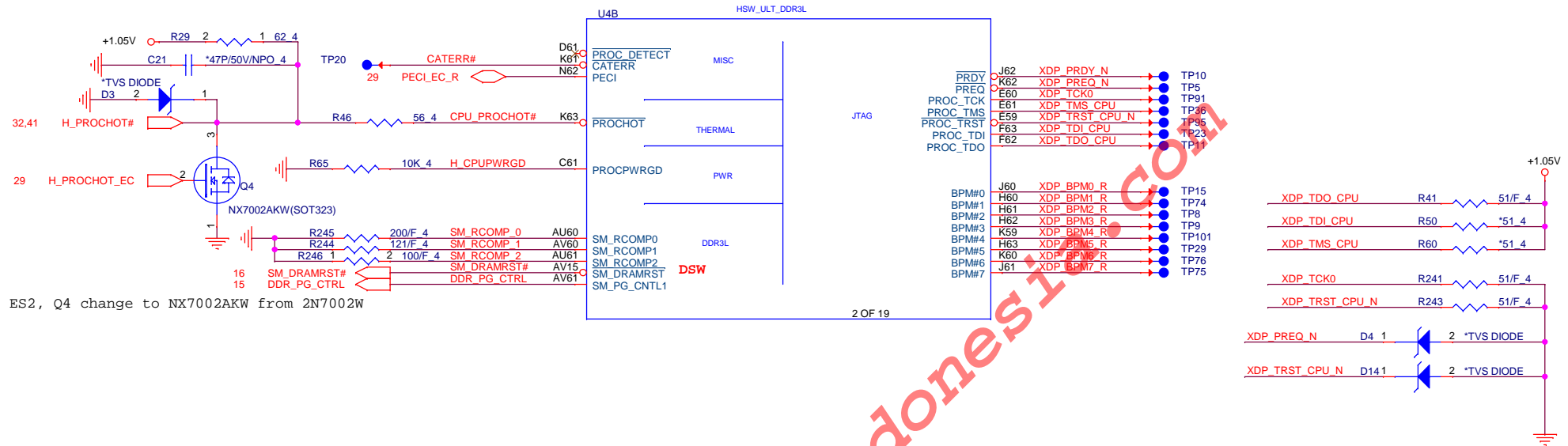
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PROJECT : MY5

HSW MCP(CFG)

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		A

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1.Level 1 Environment-related Substances Should Never be Used.
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PROJECT : MY5

Size	Document Number	Rev A
HSW MCP(Sideband)		
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CPU VDDQ

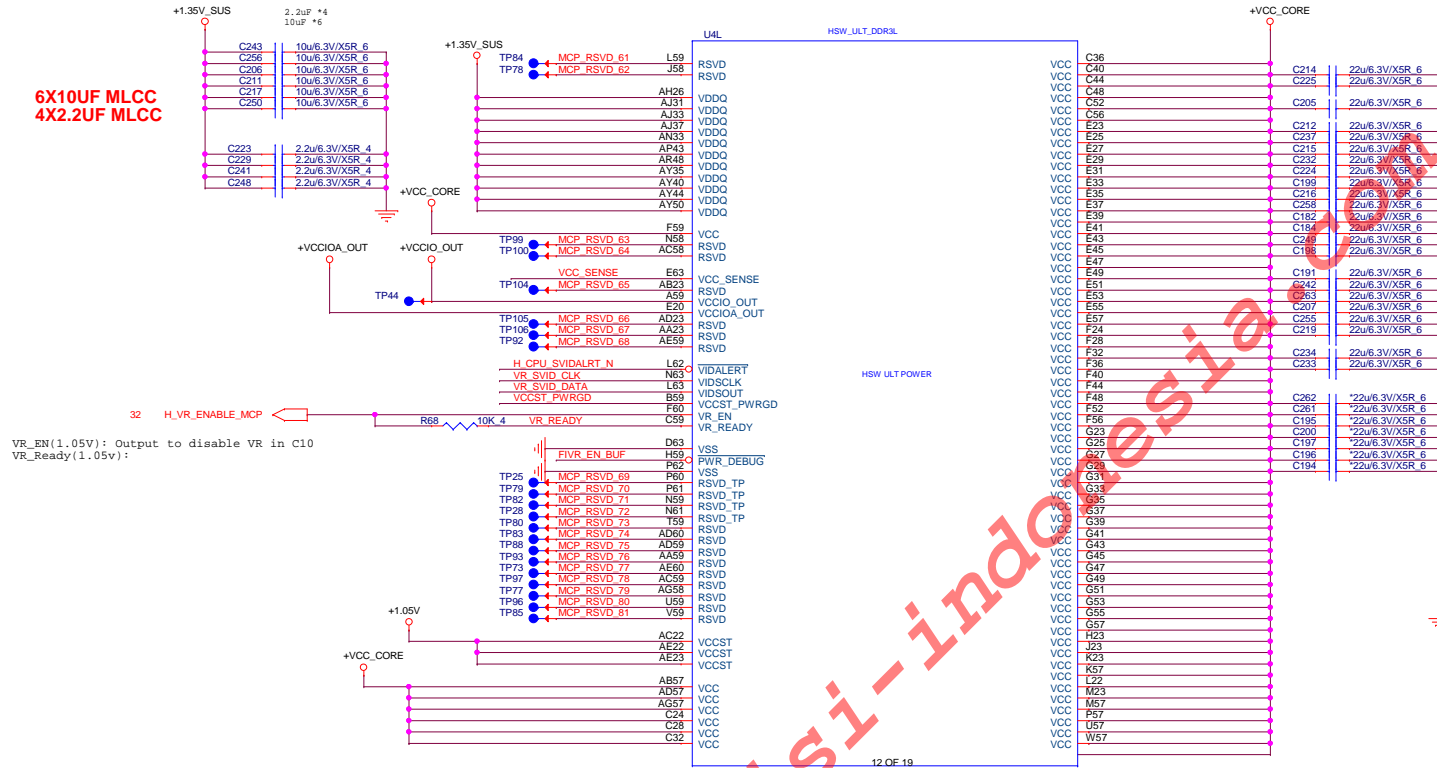
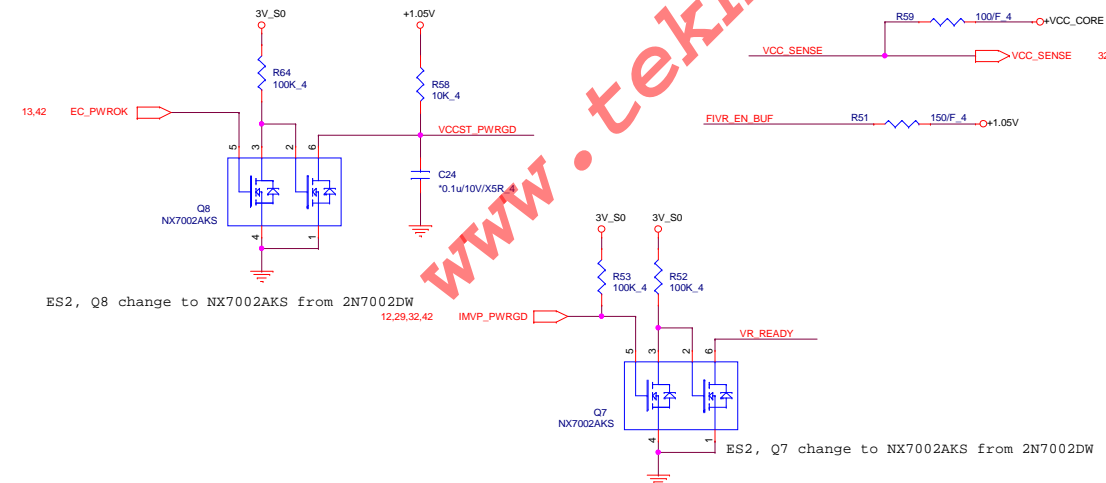
Haswell ULT 15W : 4.2A

Haswell ULT MCP (POWER)

CPU VCC

Haswell ULT 15W : 32A

23 X 22UF(0805 MLCC)

VCCST_PWRGD(O/D Input):
VCC/VDDQ/CLK stableVR_EN(1.05V): Output to disable VR in C10
VR_Ready(1.05v):

ES2, Q8 change to NX7002AKS from 2N7002DW

12,29,32,42

IMVP_PWRGD

ES2, Q7 change to NX7002AKS from 2N7002DW

SVID ALERT

close to CPU

SVID DATA

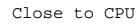
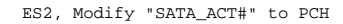
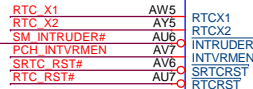
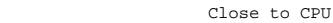
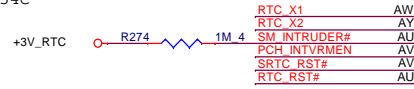
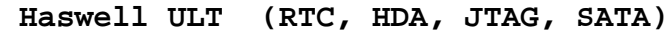
close to CPU

SVID CLK

close to VR

close to VR

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MP remove(Intel)

PP, R37, R30, R38, ~~R39~~, ~~R33~~, R36
and R40 change to Nu-Stuff

PCH Strap Table

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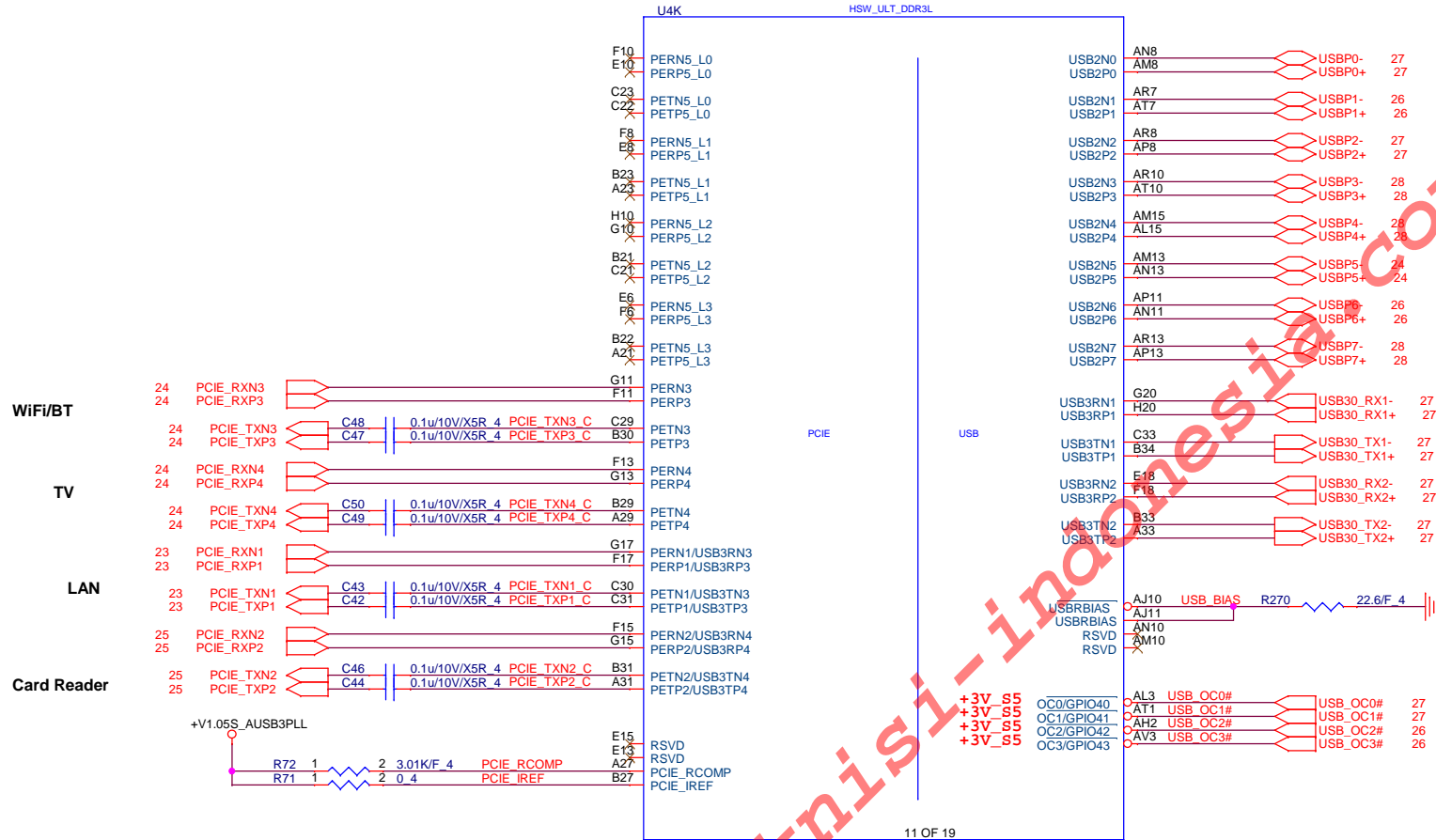
PROJECT : MY5

HSW PCH(RTC/HDA/SATA)

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	HSW PCH(RTC/HDA/SATA)	A
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Haswell ULT (PCIE,USB)

10



USB3.0 Port 1 with Charge

USB2.0 Port 1

USB3.0 Port 2

Touch Screen (Full Speed)

CAMERA

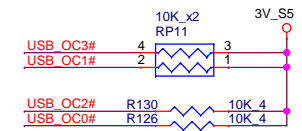
BT

HUB

RF Receiver

USB3.0 Port 1

USB3.0 Port 2

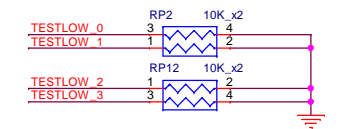


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PROJECT : MY5

Size	Document Number	Rev
	HSW PCH(PCIE/USB)	A
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- 1.Level 1 Environment-related Substances Should Never be Used.
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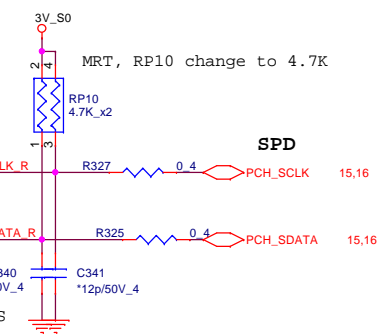
11




```
to "+V1.05S_AXCK_LCPLL" from "+1.05V"
```

The schematic diagram shows the I2C bus for the ADXL345. The bus lines are labeled PCH_SMB0_ALERT#, PCH_SMB_ALERT#, SINSR_HDR_SMALEART1, SML0CLK, and SML0DATA. The bus is terminated at the 3V_S5 supply. The termination resistors are labeled R100, R110, R92, R102, and R108. The values of the resistors are 10K 4, 10K 4, 10K 4, 2.2K 4, and 2.2K 4 respectively.

SMBus/Pull-up(CLG)



 Quanta Computer Inc. PROJECT : MY5		Rev A
Document Number	HSW PCH(CLK/LPC/SPI/SMB)	
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Hasswell ULT(GPIO,LPIO,MISC)

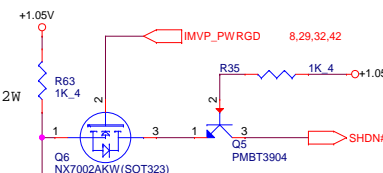
GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

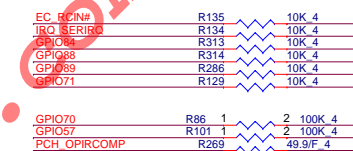
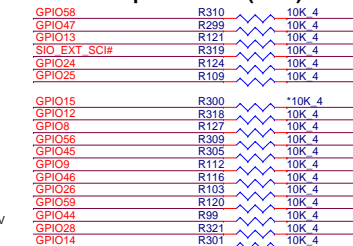
GPIO27 Deep Sx



ES2, Q6 change to NX7002AKW from 2N7002W



GPIO Pull-up/Pull-down(CLG)

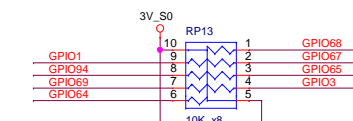


Internal PD(BIOS strap)

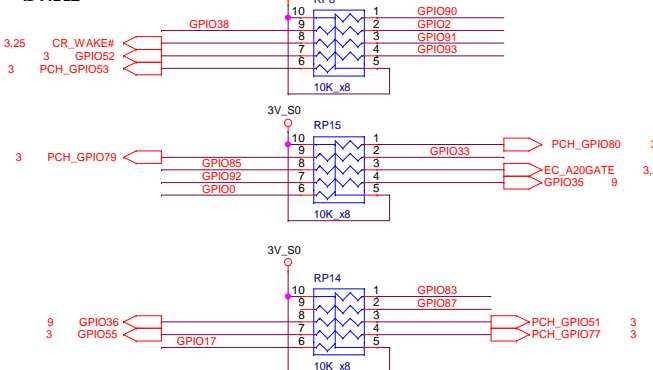
GPIO86 (BBS)	
PU	LPC
PD	SPI (Default IPD)

+V3.3S_1.8S_LPSS_SDIO R85 *1K 4 GPIO66 Internal PD

GPIO66	
R1547	ENABLE
R1547_NC	DISABLE(Default)



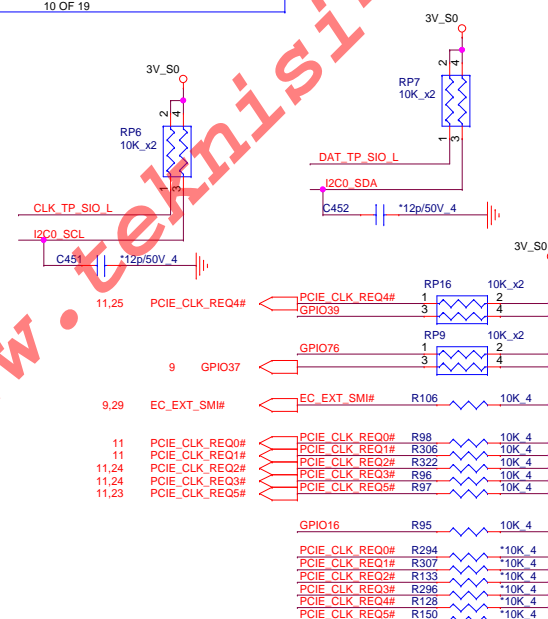
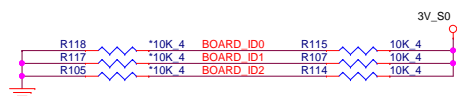
SWAP



No Reboot Strap(GPIO81)	
NC	Default
PU	EN

TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

	BOARD_ID0	BOARD_ID1	BOARD_ID2
EVT	1	1	1
w/ TV (from MRT)	1	1	1
w/o TV (from MRT)	0	1	1

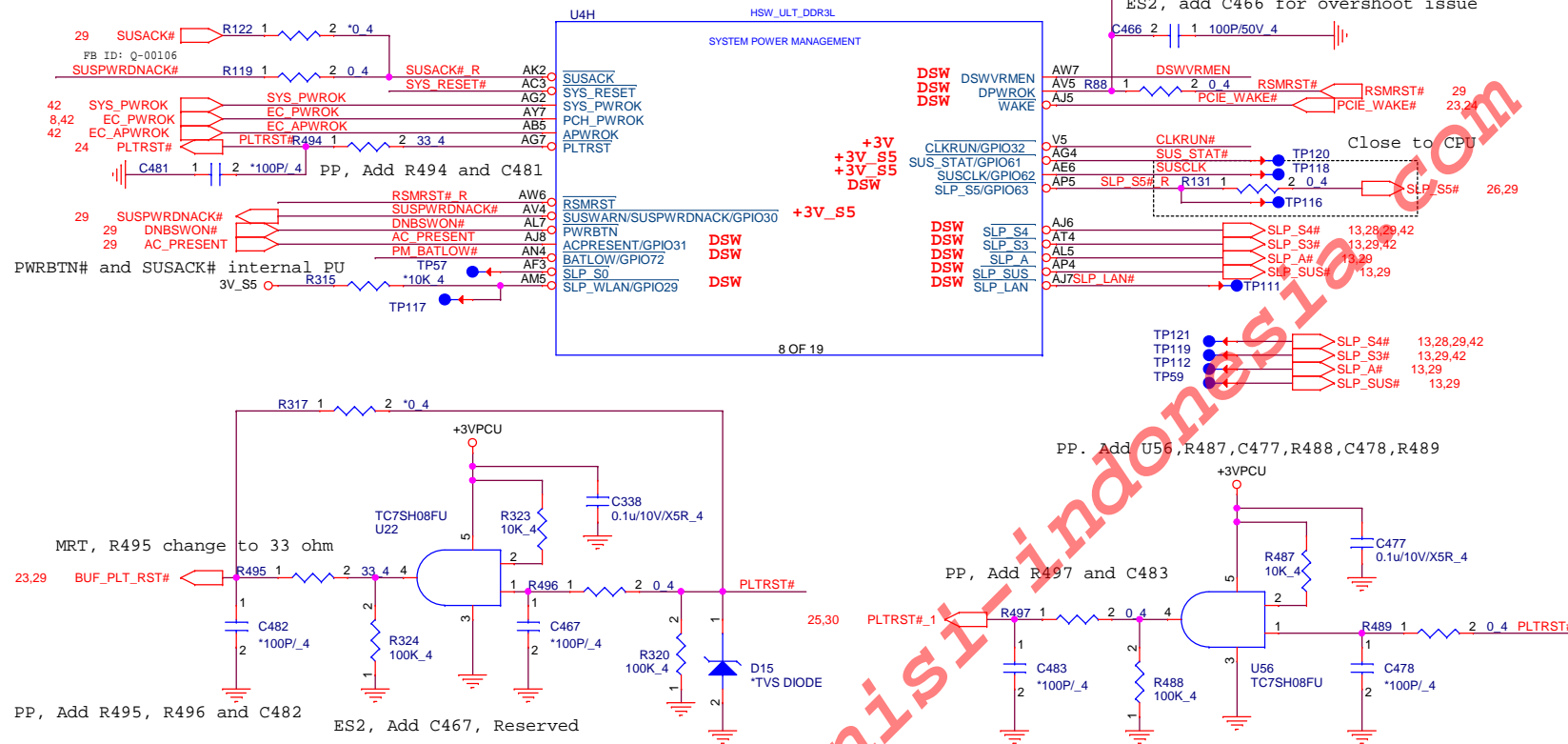


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Haswell ULT (SYSTEM POWER MANAGEMENT)

ES2, Add off page symbol for "PLTRST#"

MRT, R494 change to 33 ohm



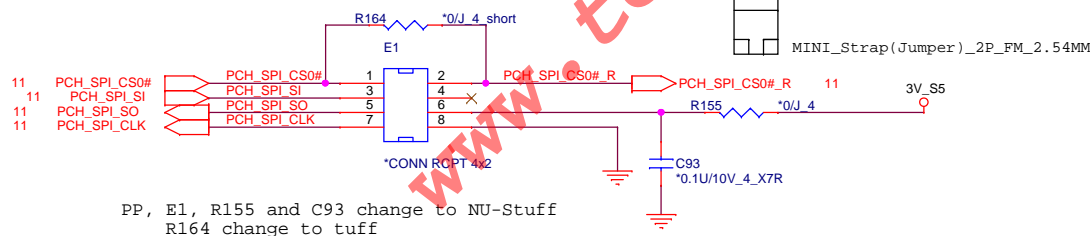
ROM recovery

MRT, R164 change to short pad

E1 (1-2)

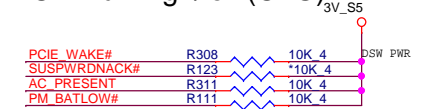
Normal, put a jumper on E1 pin 1 and pin 2

BIOS data broken, remove jumper and connect fixture to E1

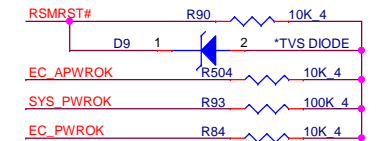
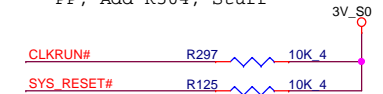


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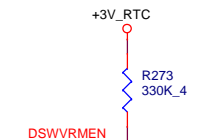
PCH Pull-high/low(CLG)



PP, Add R504, Stuff



PP, R84 Stuff



```
On Die DSW VR Enable
```

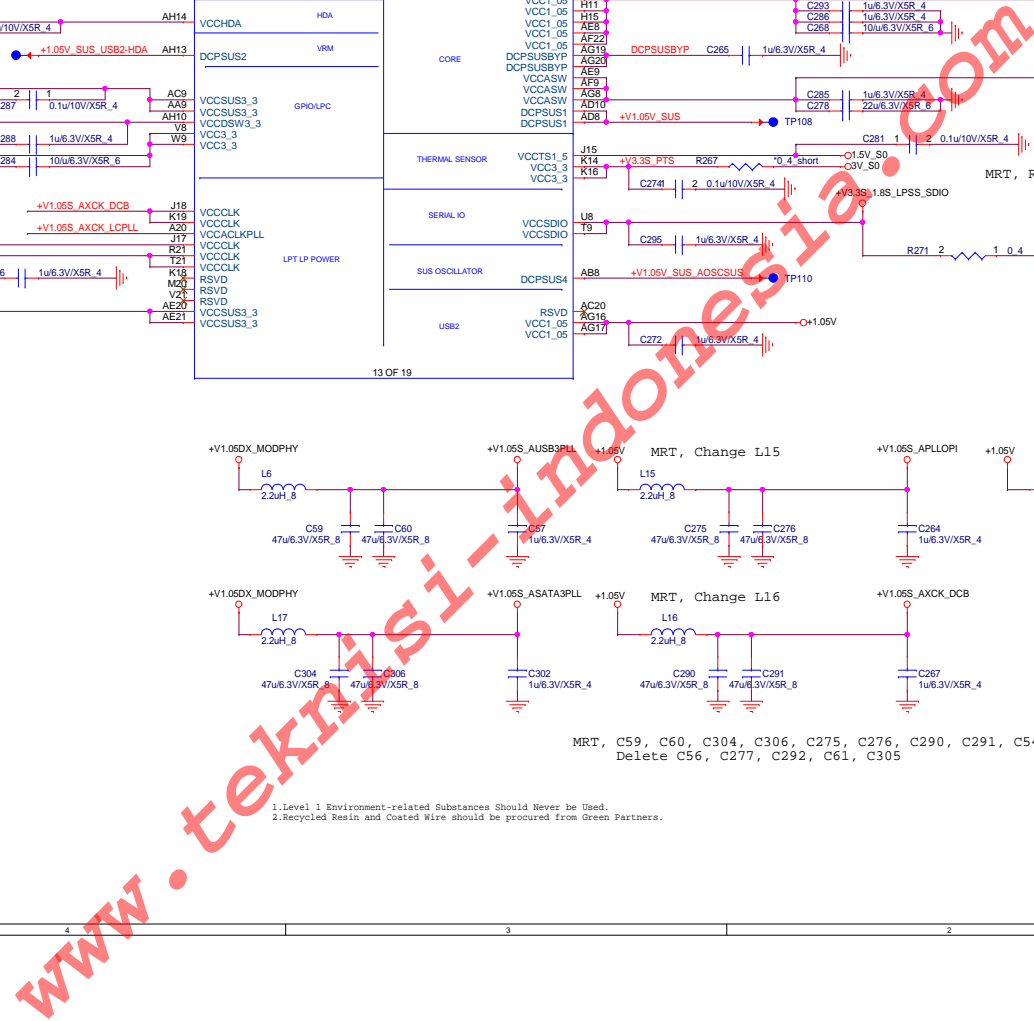
High = Enable (Default)

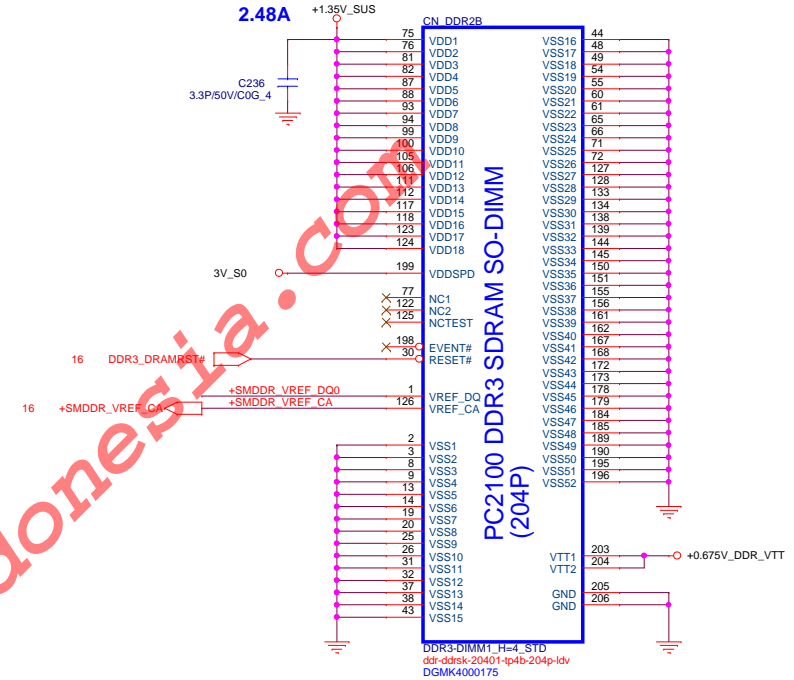
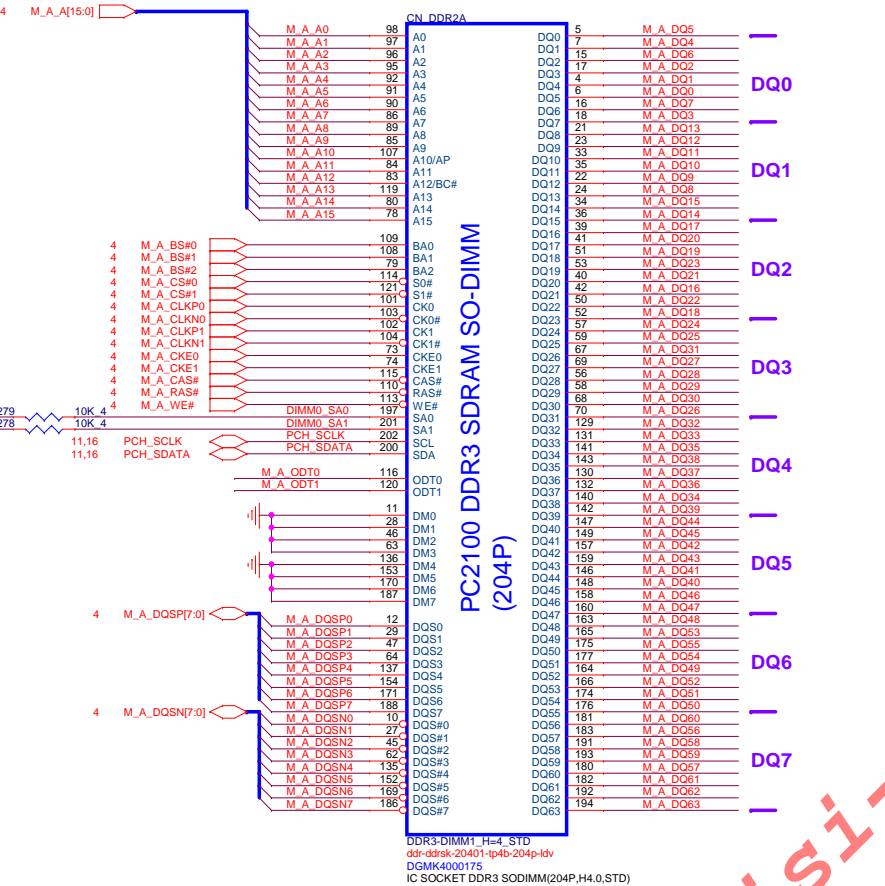
Low = Disable

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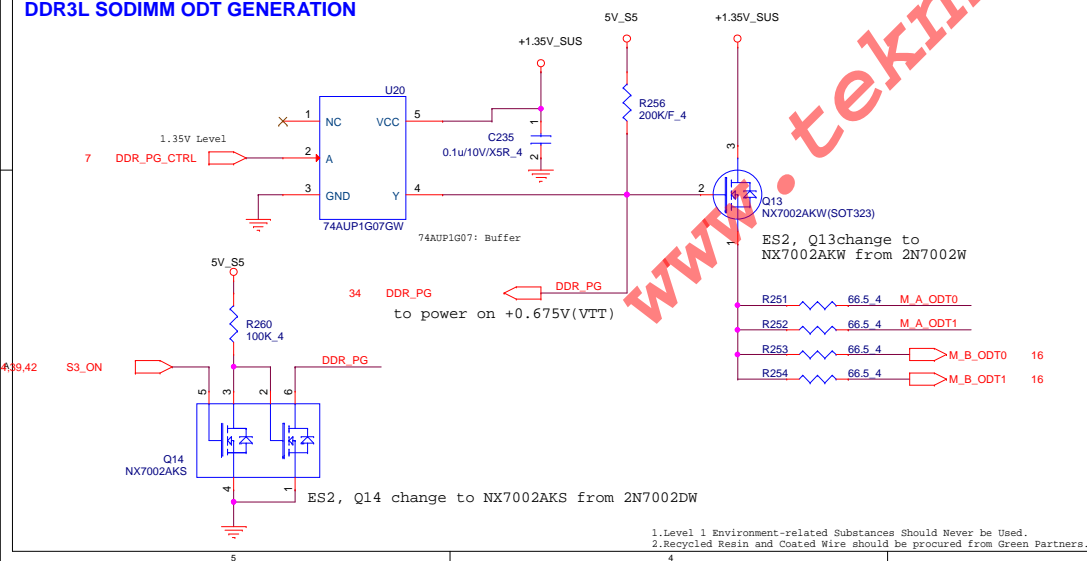
PROJECT : MY5

Size	Document Number HSW PCH(Power Management)	Rev A
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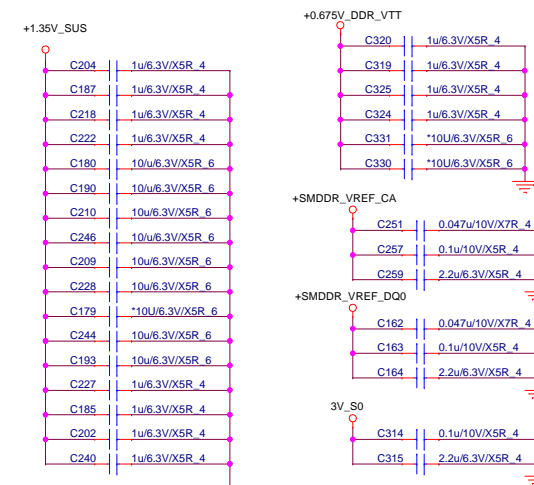




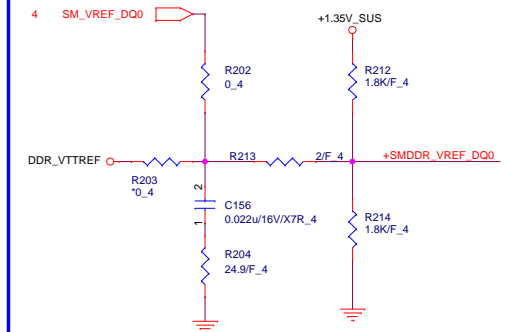
DDR3L SODIMM ODT GENERATION

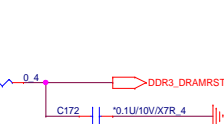


Place these Caps near So-Dimm0.



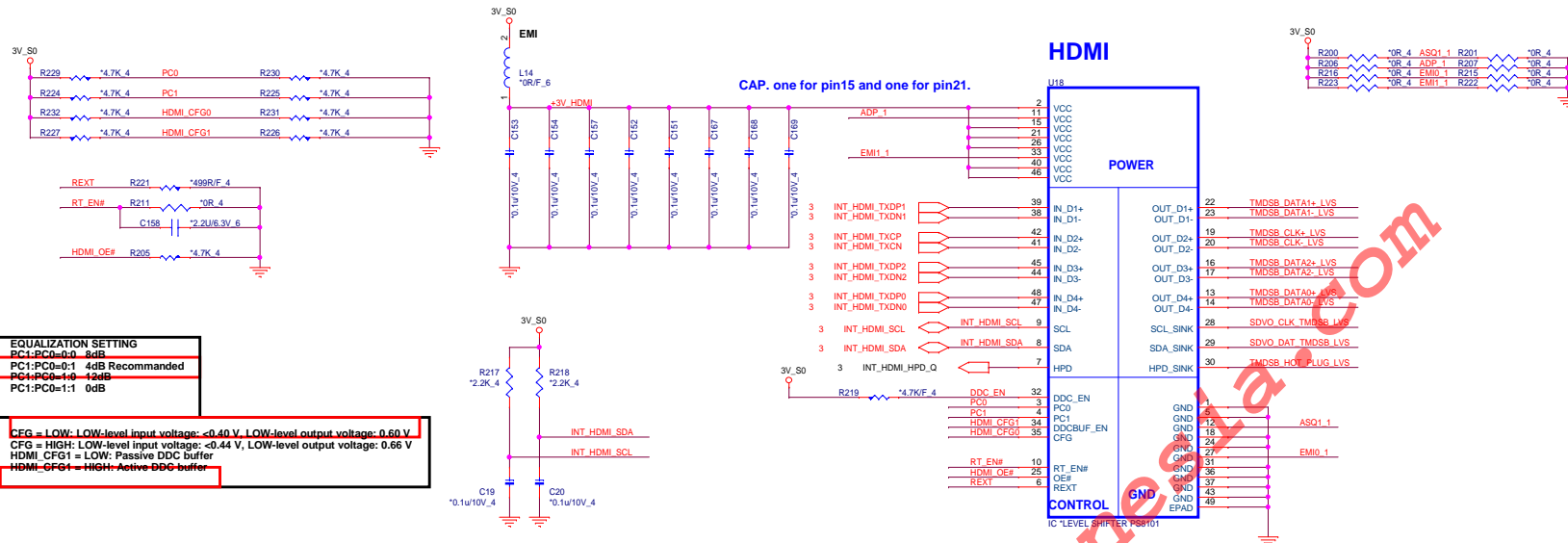
VREF DQ0 M1/M3 Solution





The schematic diagram illustrates the power supply network for the STM32F407VGT6. It shows the following rails and components:

- 1.35V_SUS:** A rail with decoupling capacitors C230 through C247, all with values of 1u6.3V/XSR_4 or 10u6.3V/XSR_6.
- +0.675V_DDR_VTT:** A rail with decoupling capacitors C329 through C337, all with values of 1u6.3V/XSR_4 or 10u6.3V/XSR_6.
- +SMDDR_VREF_CA:** A rail with decoupling capacitors C252, C254, and C253, with values of 0.047u10V/XTR_4, 0.1u10V/XSR_4, and 2.2u6.3V/XSR_4 respectively.
- +SMDDR_VREF_DQ1:** A rail with decoupling capacitors C159, C160, and C161, with values of 0.047u10V/XTR_4, 0.1u10V/XSR_4, and 2.2u6.3V/XSR_4 respectively.
- 3V_S0:** A rail with decoupling capacitors C311 and C312, with values of 0.1u10V/XSR_4 and 2.2u6.3V/XSR_4 respectively.

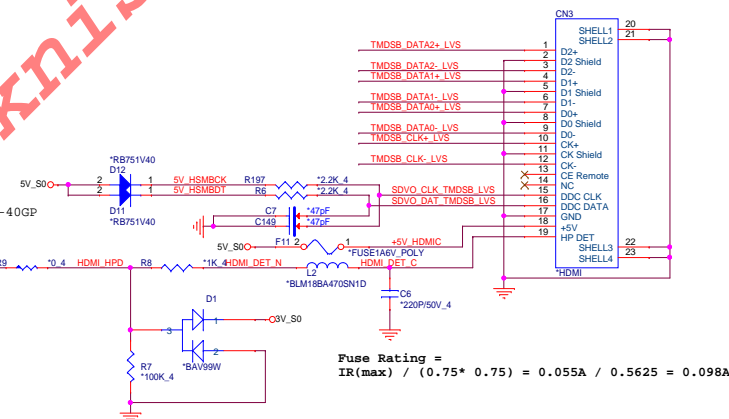
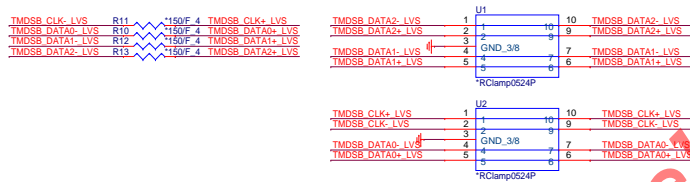


PP, Remove All HDMI components
 R229, R225, R231, R227, R221, R205, R217, R218, L14,
 C153, C154, C157, C152, C151, C167, C168, C169, R219,
 U18, R201, R206, R215, R223, D12, R197, R6, F11, R9,
 R8, R7, D1, L2, C6, C9, D11

ESD Protection

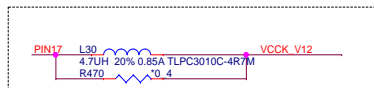
Reserve for EMI

layout note: close HDMI connector

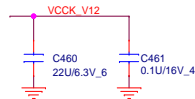


	4.7-uH(L30)	0 Ohm(R470)
SWR	Connect	NC
LDO	NC	Connect

SWR MODE

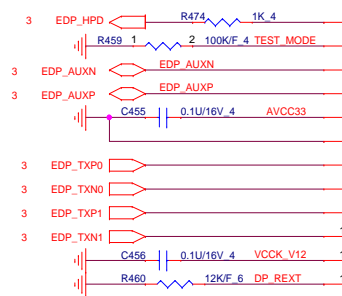


LDO MODE



1. C41 10-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN17

ES2, eDP to LVDS converter change to RTD2136R-CG



MRT, RP18 change to Nu-Staff

MRT, RP19 change to 4.7K

MRT, R476 connect to R_PCH_SDATA from SML0DATA

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

MRT, R475 connect to R_PCH_SCLK from SML0CLK

RTD2136R-CG

	MODE_CFG0(PIN47)	
	0	1
MODE_CFG1(PIN48)	0	X
	1	ROM ONLY MODE
		EEPROM MODE

EEPROM

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

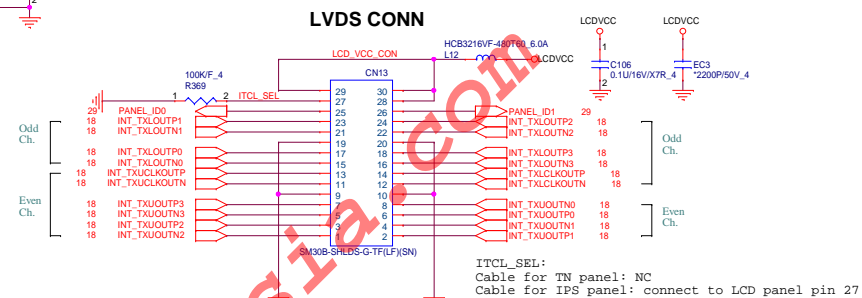
Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8

Address=0xA8



TO CONVERTER CONNECT

TO CONVERTER CONNECT

2A-80V PHEM_1206

20V_CONVERTER

100pF/50V_4

0.1uF/25V/X5R_4

4.7uF/25V_8

0.1uF/25V/X5R_4

PANEL_PWM

LCD_BLEN

CN14

LED_DRIVER_ACS(85205-0800L)

LED_ID

29

IN(max) / (0.75 * 0.75) =
8 / (0.5) / 0.5625 = 1.504A

3V3PCU

C393

0.1uH/6V/X7R_4

2

1

4

U39 TC7SH08FU

R404 10kF_4

R400 10kF_4

R398 10kF_4

R399 10kF_4

R408 10kF_4

R410 10kF_4

22.29 NIGHT_MODE#

29 BACKLIGHT_ON From EC

3.29 EDP_BKLEN From Haswell_ULI

18.29 LVDS_DISPON From ANX1122

LCD BL_EN

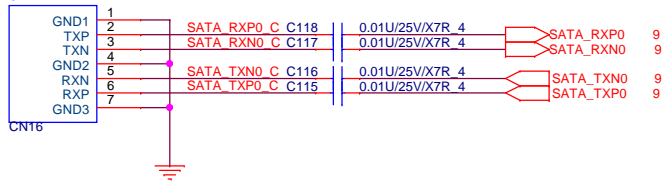
PWM CONTROL

From EC
From ANX1122
From Haswell_ULT

3.5" SATA HDD

DFHS07FR023
sata-c12712-10704-l-7p-r
SATA-HDD

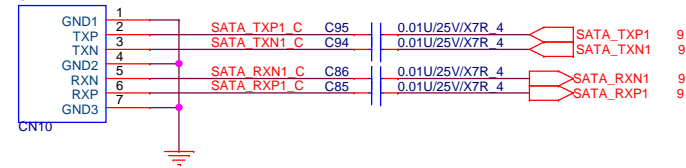
Place these SATA AC Cap close to device , not PCH



SATA ODD

DFHS07FR023
sata-c12712-10704-l-7p-r
SATA-HDD

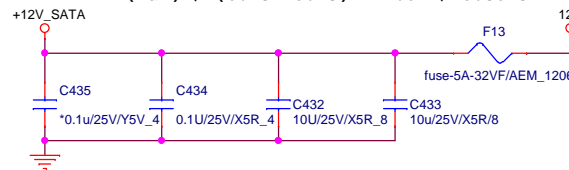
Place these SATA AC Cap close to device , not PCH



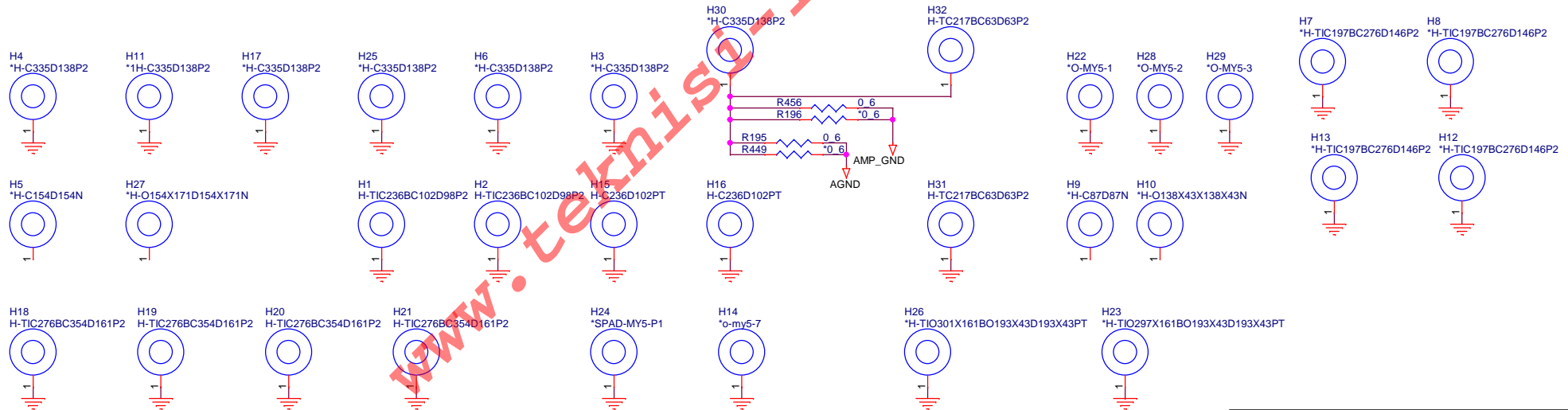
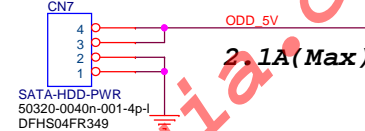
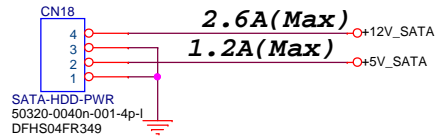
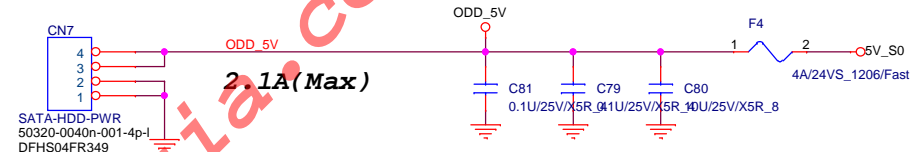
$$\text{Fuse Rating} = \frac{\text{IR(max)}}{(0.75 * 0.75)} = \frac{1.2A}{0.5625} = 2.13A$$



$$\text{Fuse Rating} = \frac{\text{IR(max)}}{(0.75 * 0.75)} = \frac{2.6A}{0.5625} = 4.62A$$



$$\text{Fuse Rating} = \frac{\text{IR(max)}}{(0.75 * 0.75)} = \frac{2.1A}{0.5625} = 3.733A$$



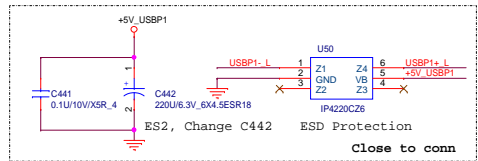
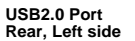
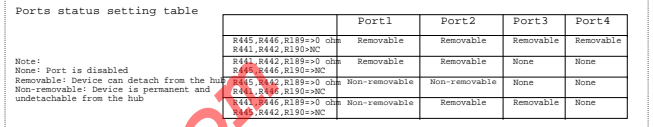
Quanta Computer Inc.

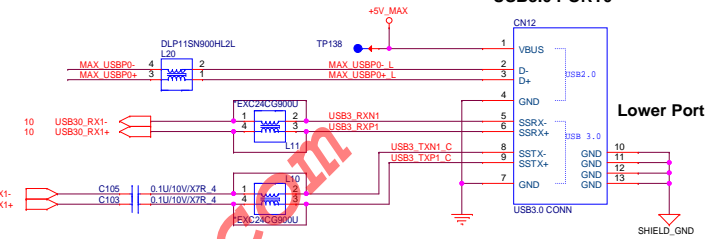
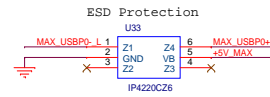
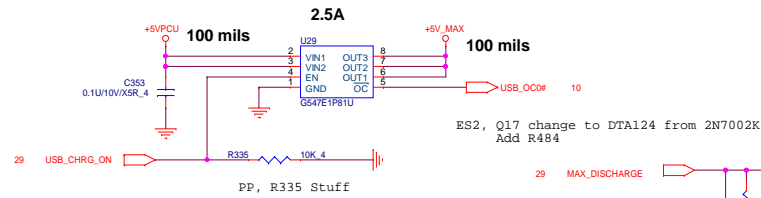
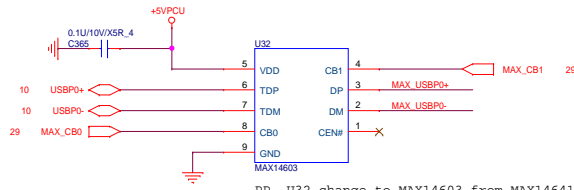
PROJECT : MY5

Size	Document Number	Rev
	HDD/ODD	A

Date: Wednesday, October 23, 2013 Sheet 20 of 46



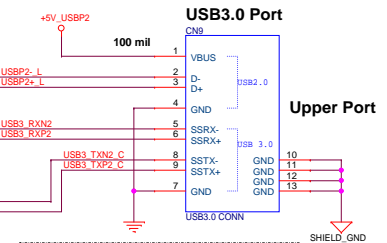
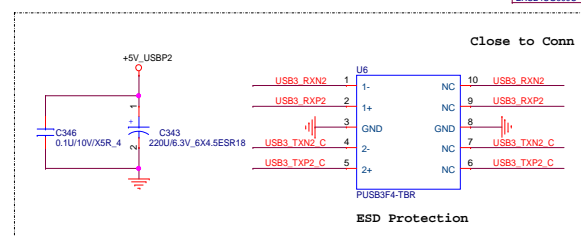
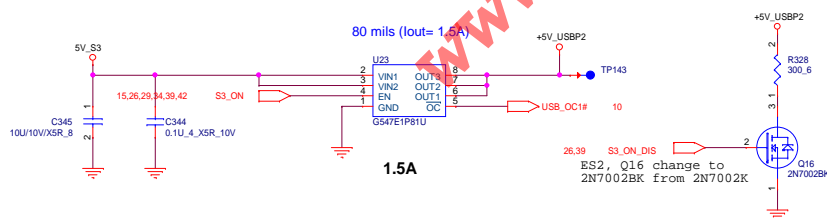




USB Charger Enable						
Power State	Mode	CB0	CB1	USB_CHRG_ON	MAX_DISCHARGE	Power Source
S0	PM	1	0	1->0->1	0->1->0	AC
S3	AM	0	0	1->0->1	0->1->0	AC*1
S4/S5	AM	0	0	1->0->1	0->1->0	AC*1
G3->S5						Base on AC
USB Charger Disable						
Power State	Mode	CB0	CB1	USB_CHRG_ON	MAX_DISCHARGE	Power Source
S0	PM	1	0	1	0	AC
S3	PM	1	0	1	0	AC
S4/S5	PM	1	0	0	1	AC
G3->S5						Base on AC

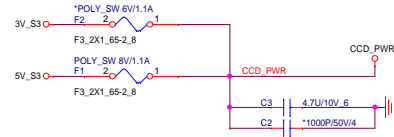
*1 : Discharge min. 700ms

CB0	CB1	Mode	Status
0	0	AM	Auto Detection Charger Mode
0	1	FM	Force Dedicated Charger Mode: DP/DM shorted
1	0	PM	USB Pass-Through Mode: DP/DM connected to TDP/TDM
1	1	CM	USB Pass-Through Mode with CDP Emulation; auto connects DP/DM to TDP/TDM depending on CDP status

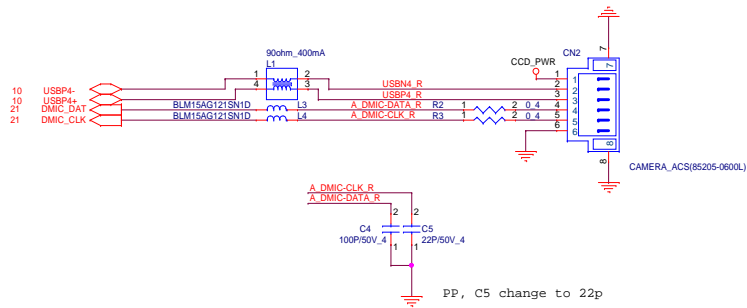


WEBCAM

$$\text{Fuse Rating} = \frac{\text{IR(max)}}{(0.75 \times 0.75)} = \frac{0.16\text{A}}{0.5625} = 0.284\text{A}$$

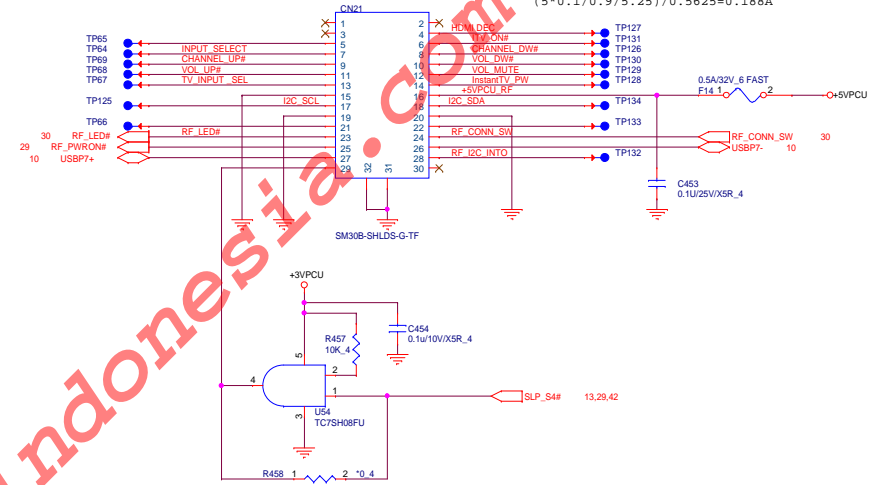


$$\text{Fuse Rating} = \frac{\text{IR(max)}}{(0.75 \times 0.75)} = \frac{0.16\text{A}}{0.5625} = 0.284\text{A}$$



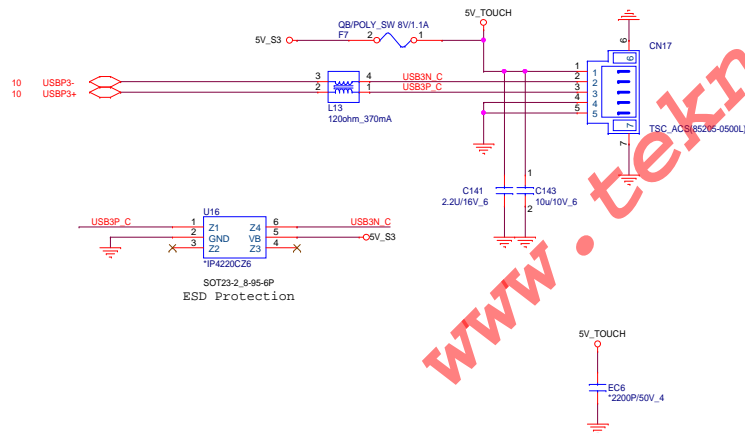
RF Board

$$\text{Fuse Rating} = \frac{\text{IR(max)}}{(0.75 \times 0.75)} = \frac{5 \times 0.1 / 0.9 / 5.25}{0.5625} = 0.188\text{A}$$

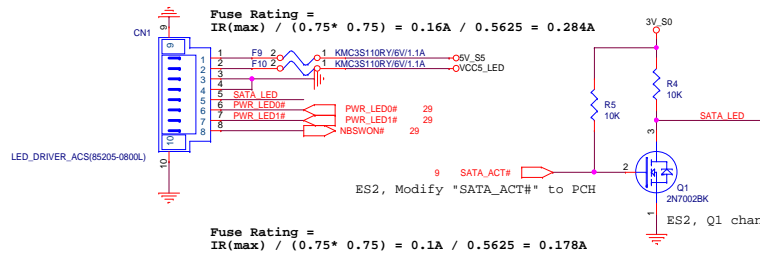


Touch Panel

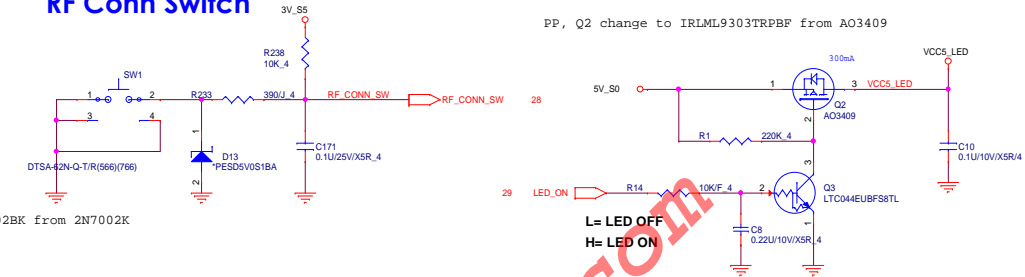
$$\text{Fuse Rating} = \frac{\text{IR(max)}}{(0.75 \times 0.75)} = \frac{0.15\text{A}}{0.5625} = 0.287\text{A}$$



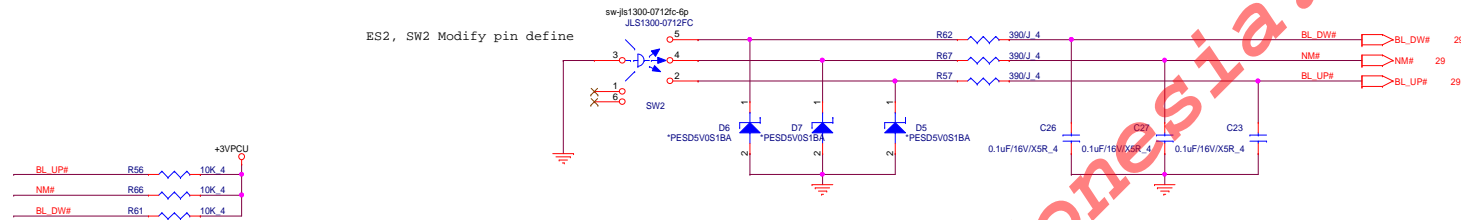
To Power Switch Board



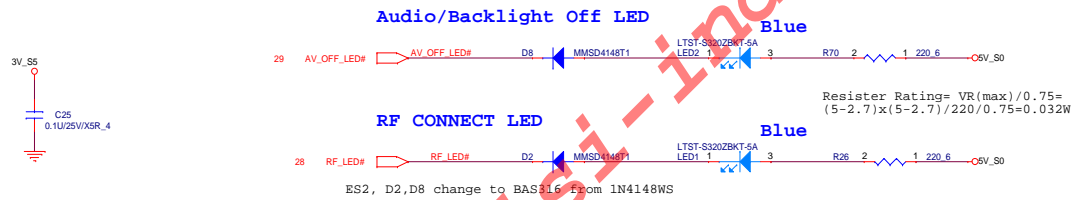
RF Conn Switch



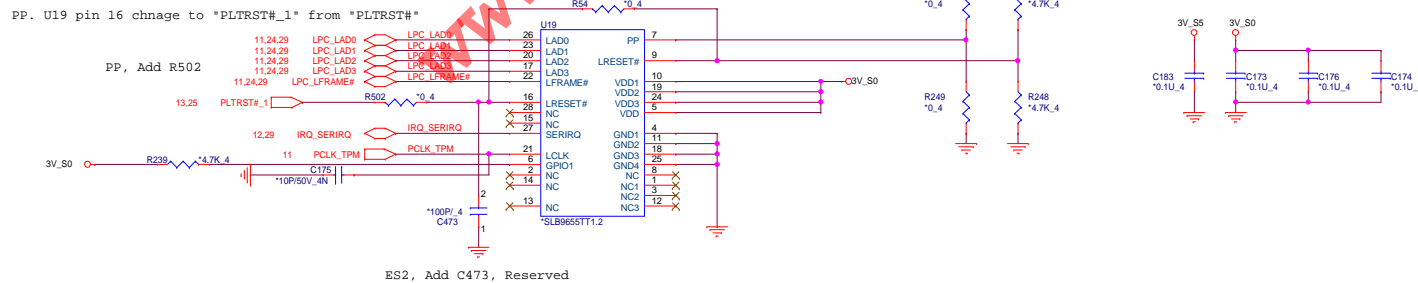
Audio/Backlight Off Switch



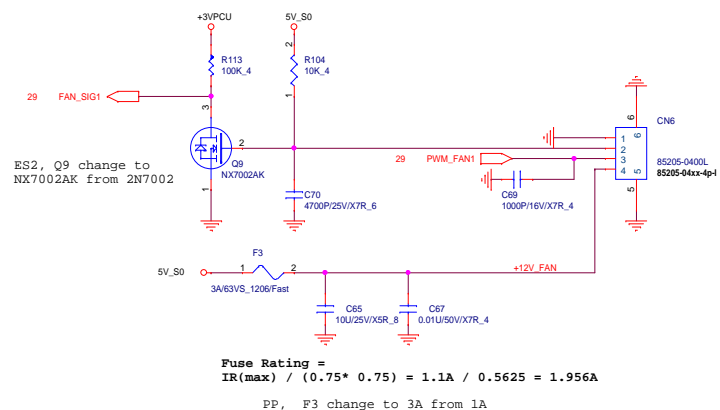
Audio/Backlight Off LED

**TPM**

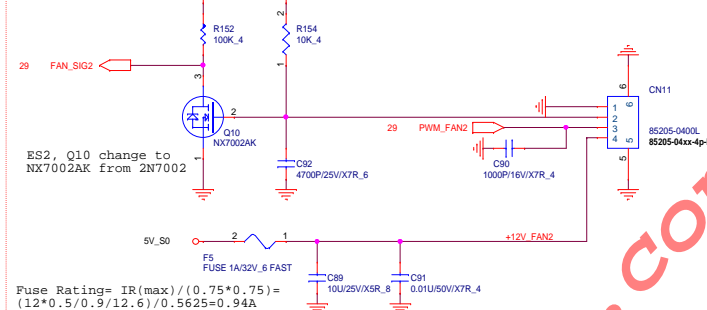
I/O Address (PCI BUS address)		
BADDR	Index	Data
0	2E	2F
1	4E	4F



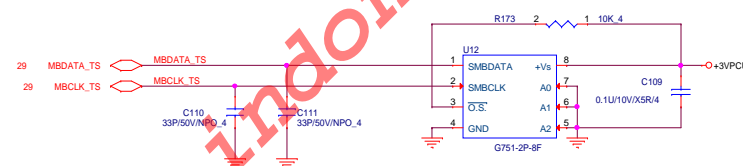
PWM FAN CTRL for 1st FAN



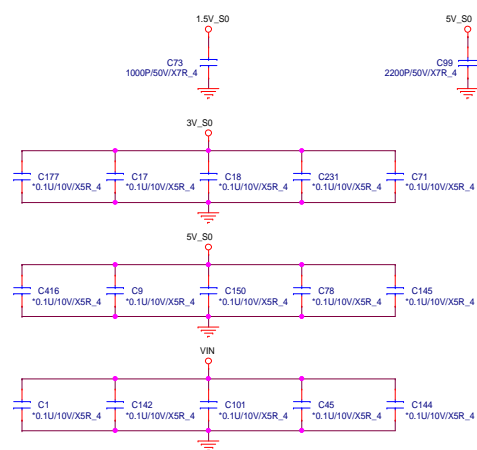
PWM FAN CTRL for 2nd FAN

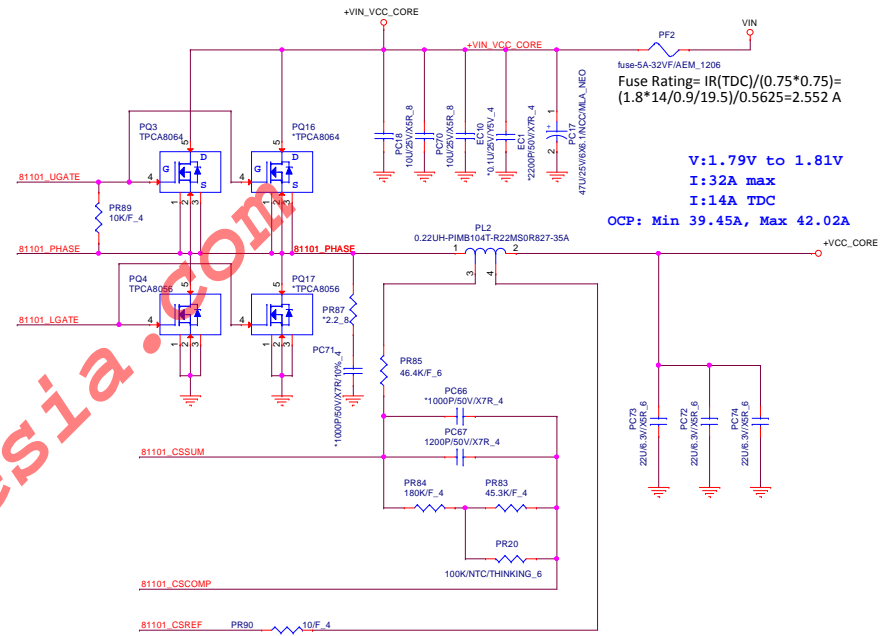


Thermal Sensor for PC-TV

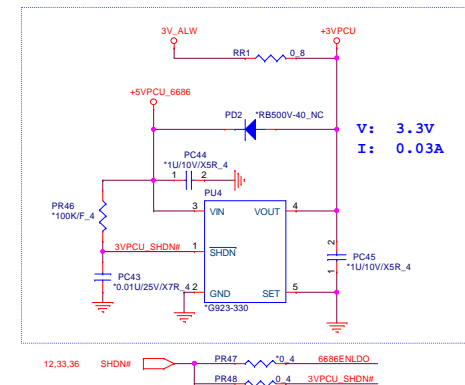
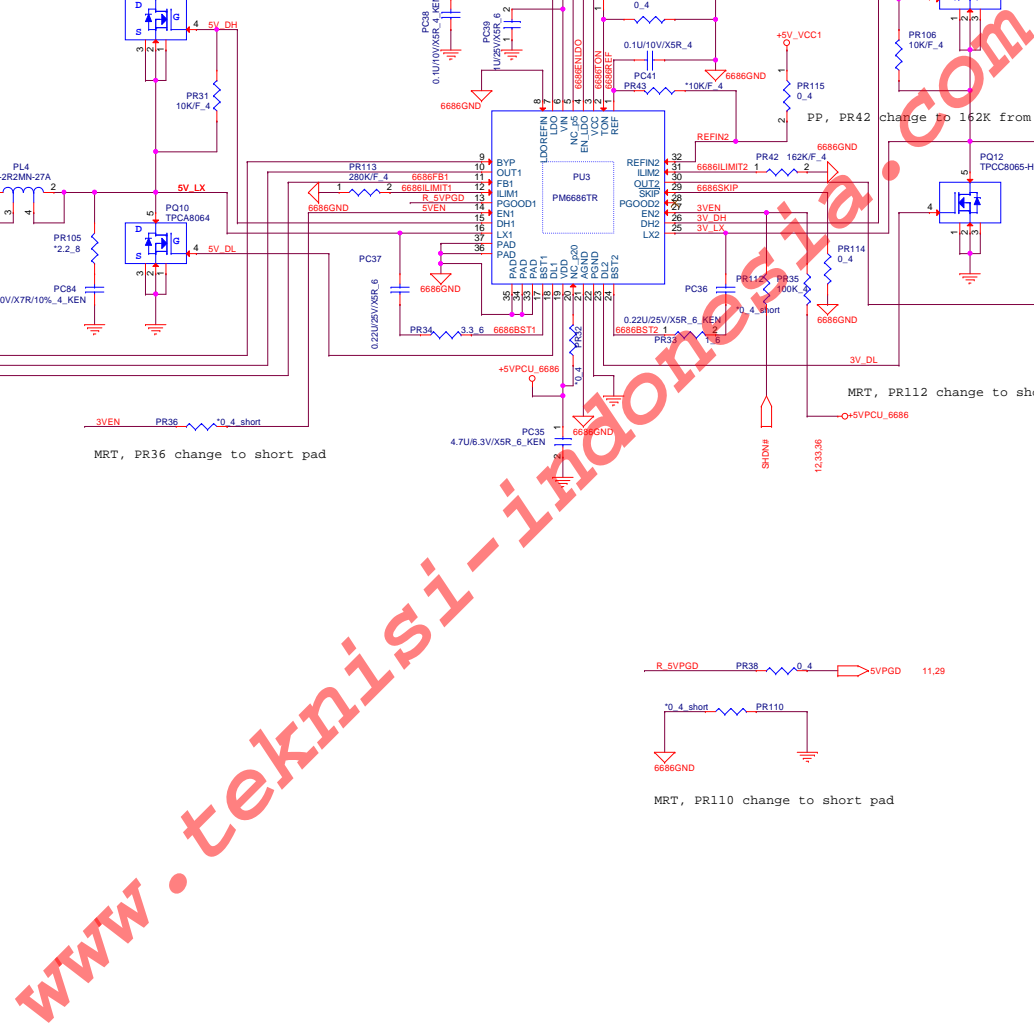


For EMI



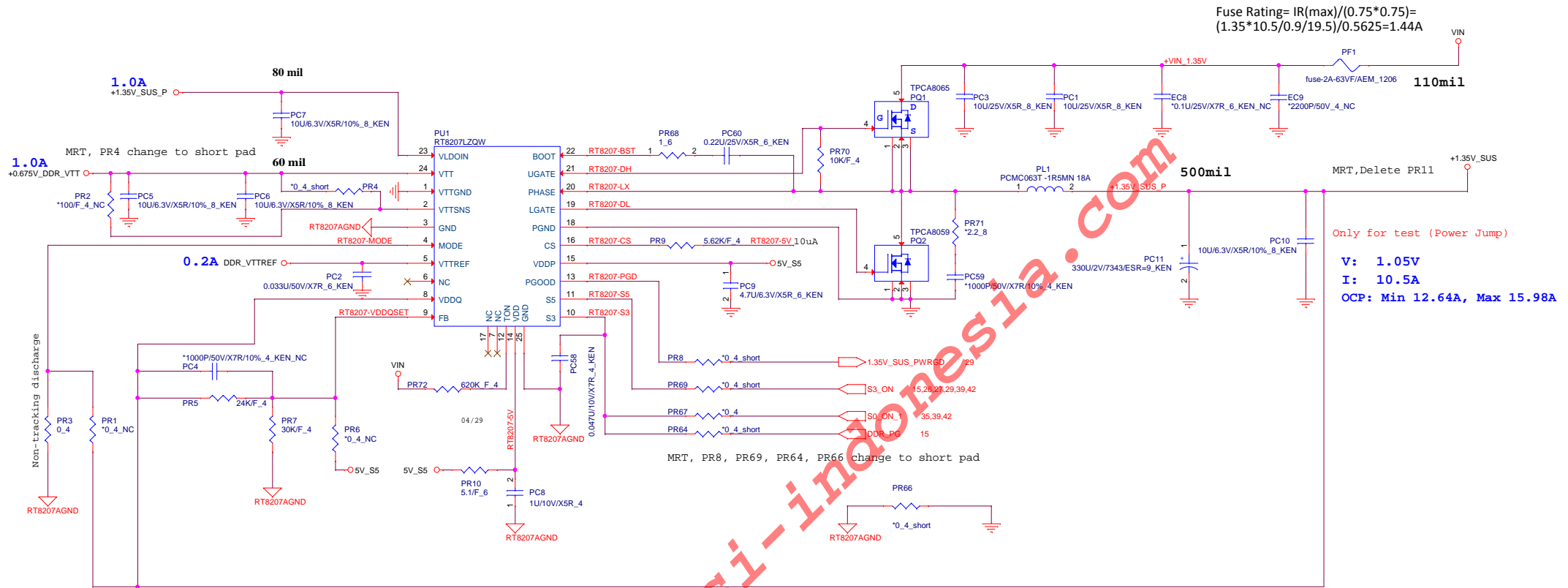


33



DDR3 1.35VSUS & DDR_VTERM (RT8207LZQW)

34

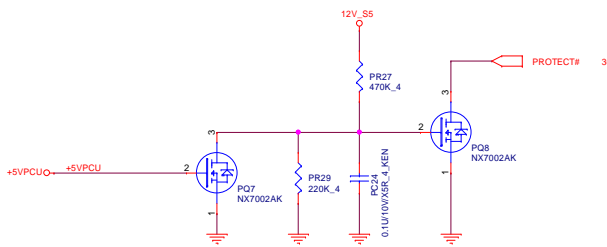
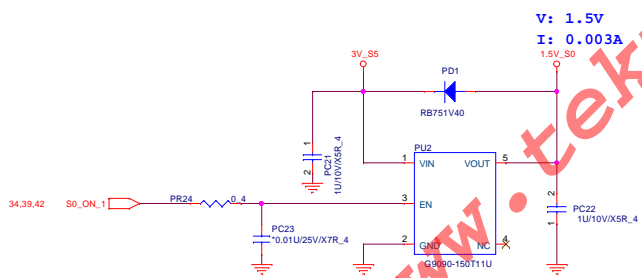
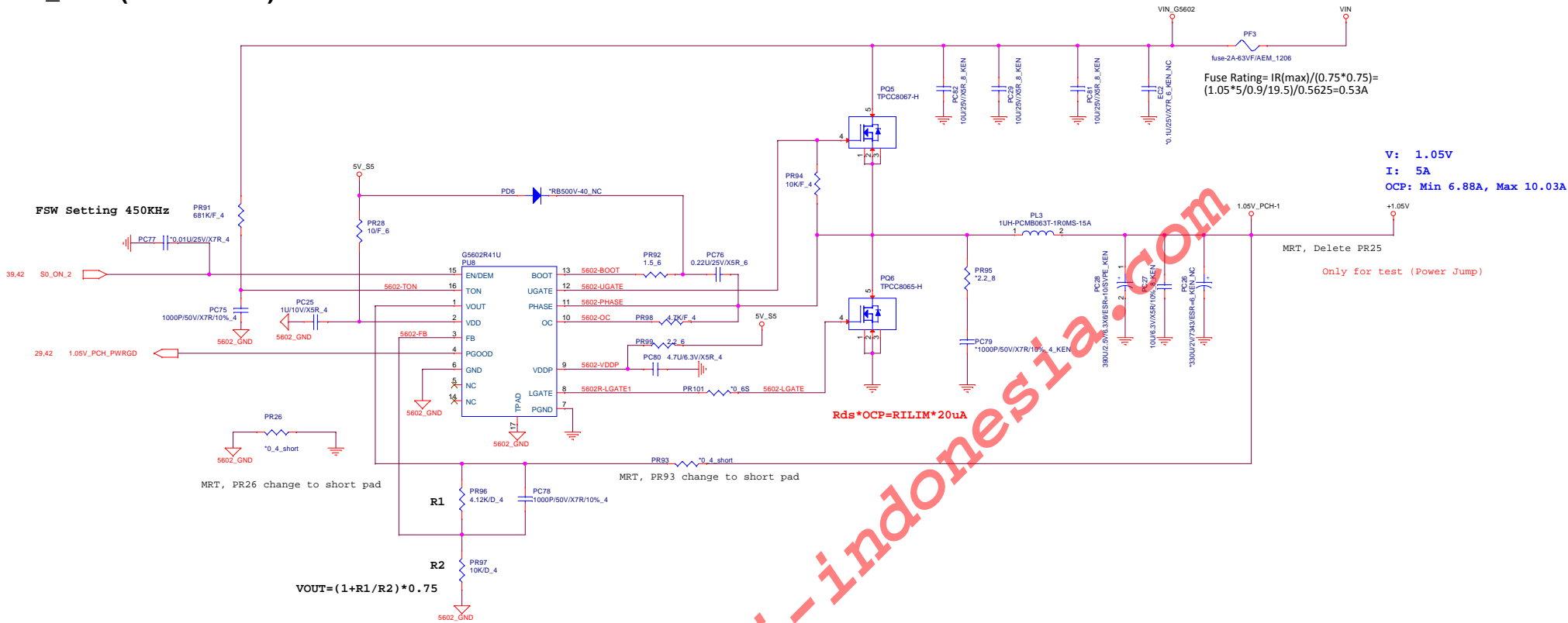


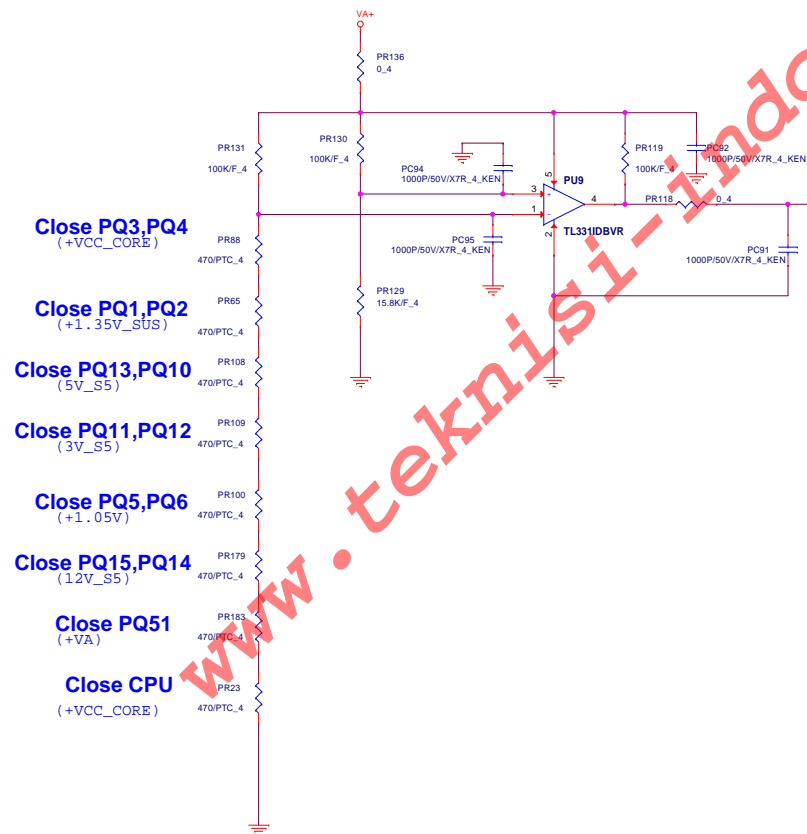
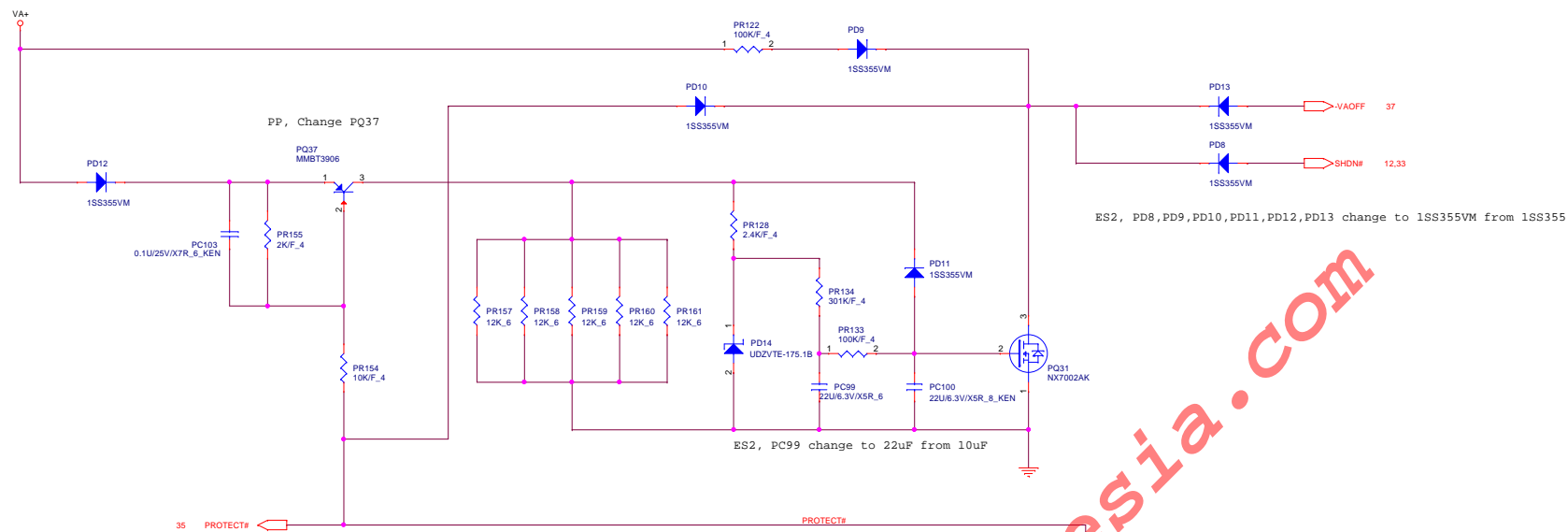
MODE	DISCHARGE MODE
+5V	No discharge
+1.35V	Tracking discharge
GND	Non-tracking discharge

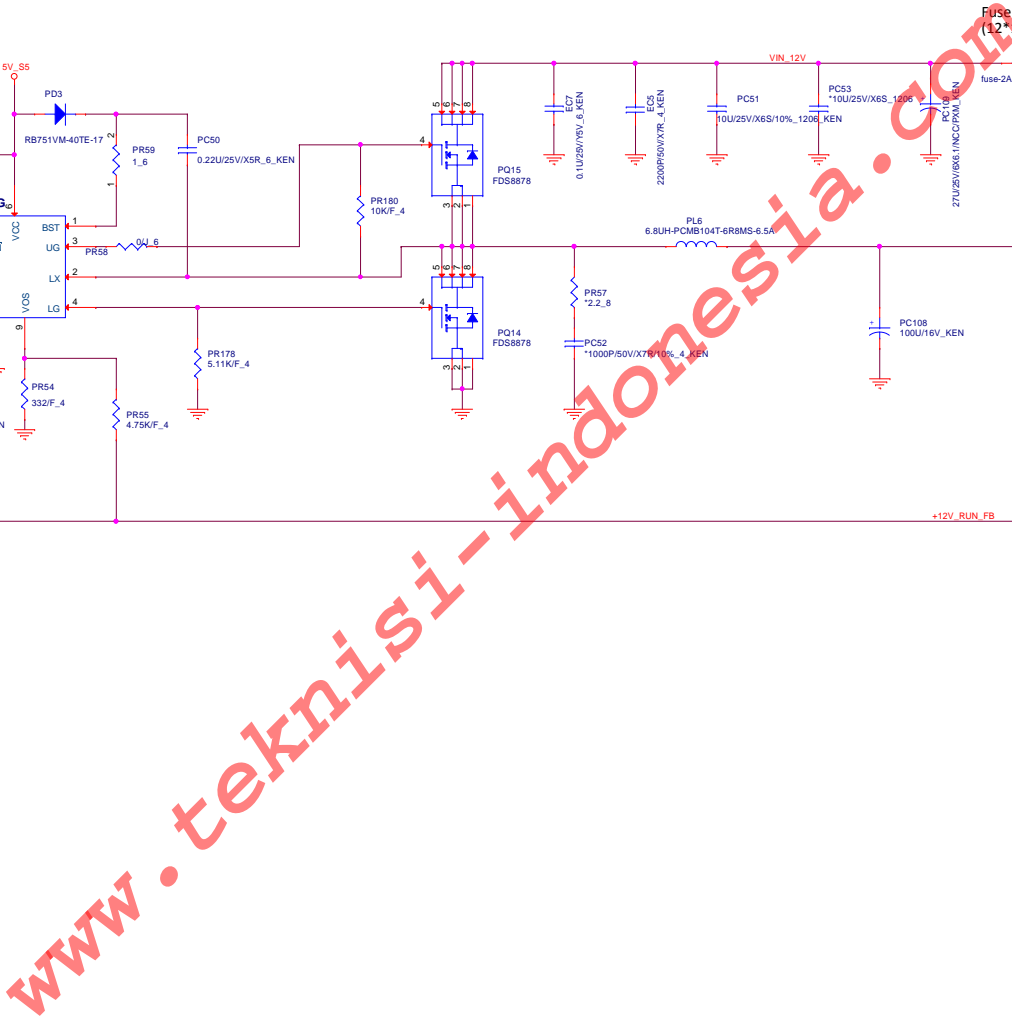
VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.2V<VDDQ<3V

$$VTT = VTTREF = VDDQSNS/2 = 0.675V$$

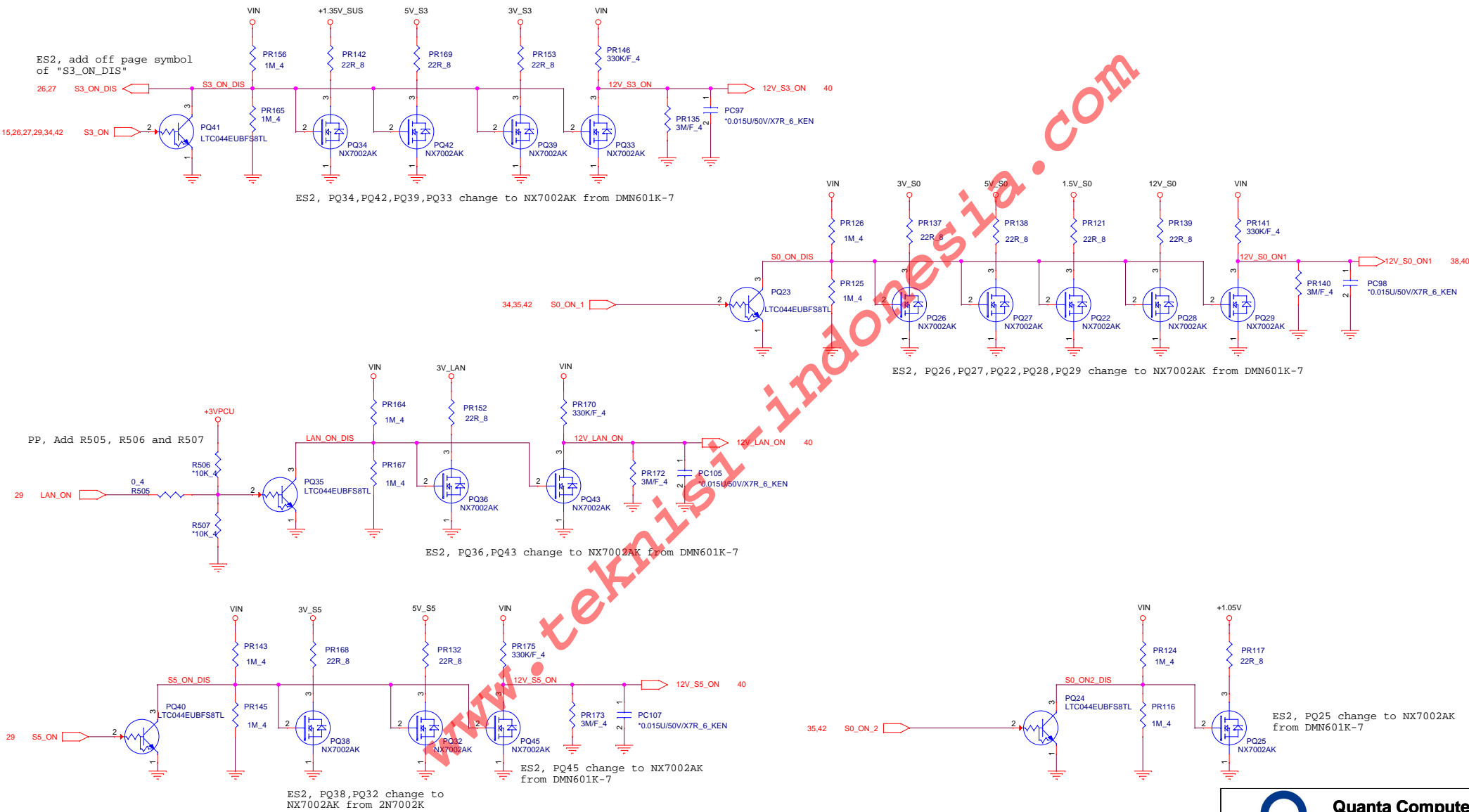
STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off



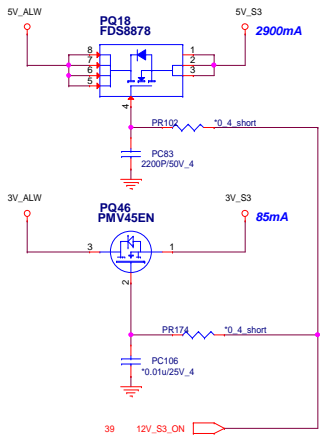




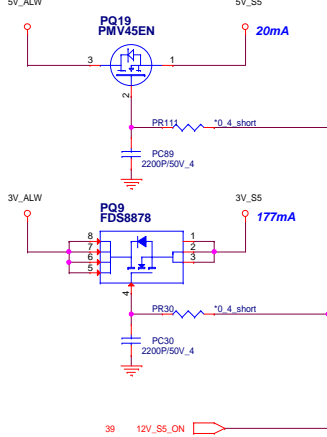
V: 12V
I: 1A
OCP: Min 2.3A, Max 4.12A



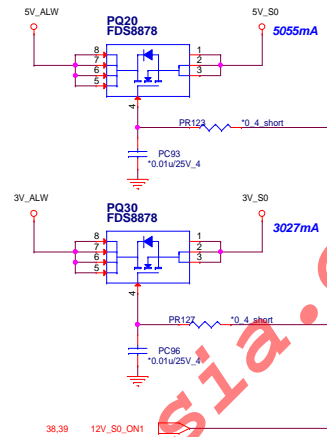
S3 ON Load SW



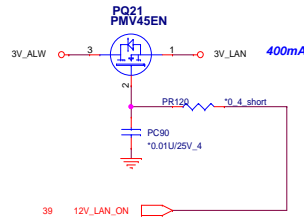
S5 ON Load SW



S0 ON1 Load SW



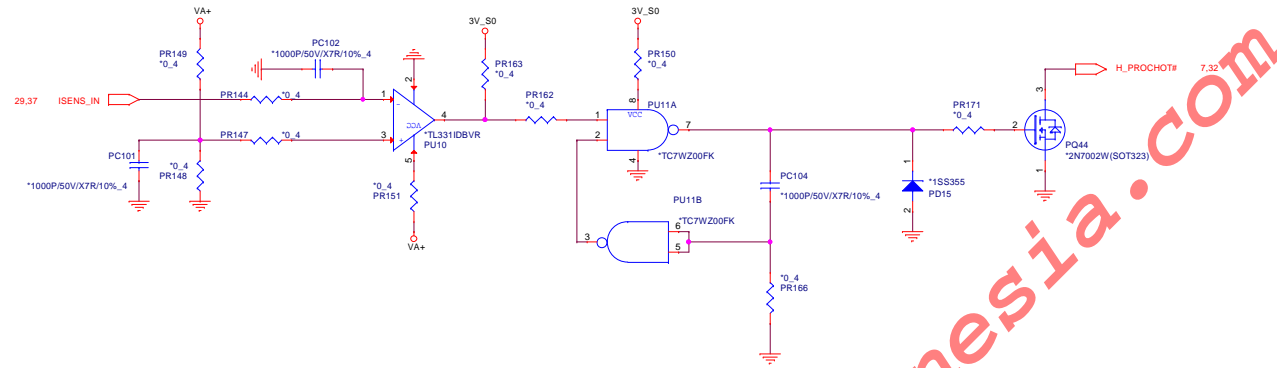
LAN_ON Load SW

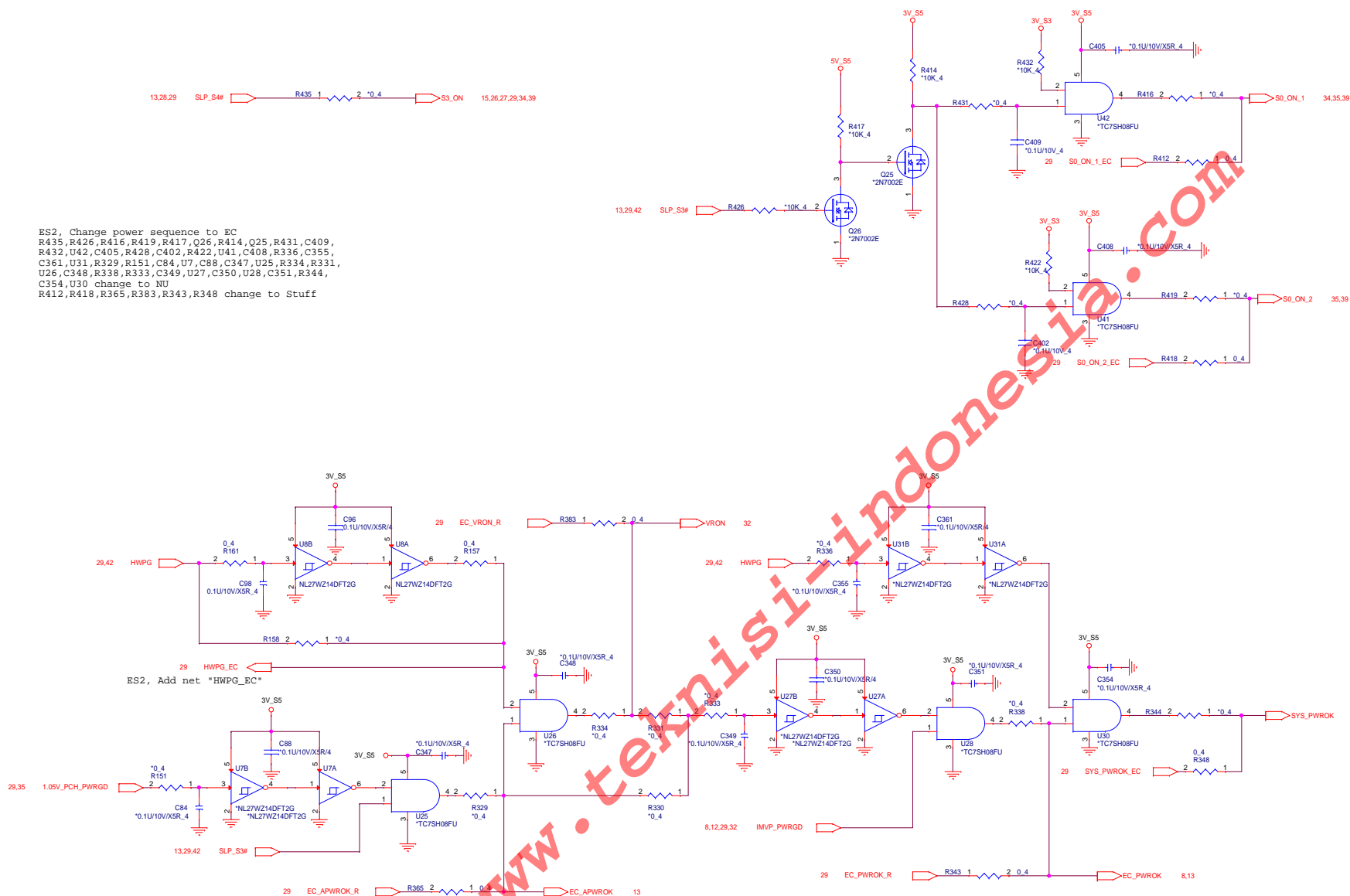


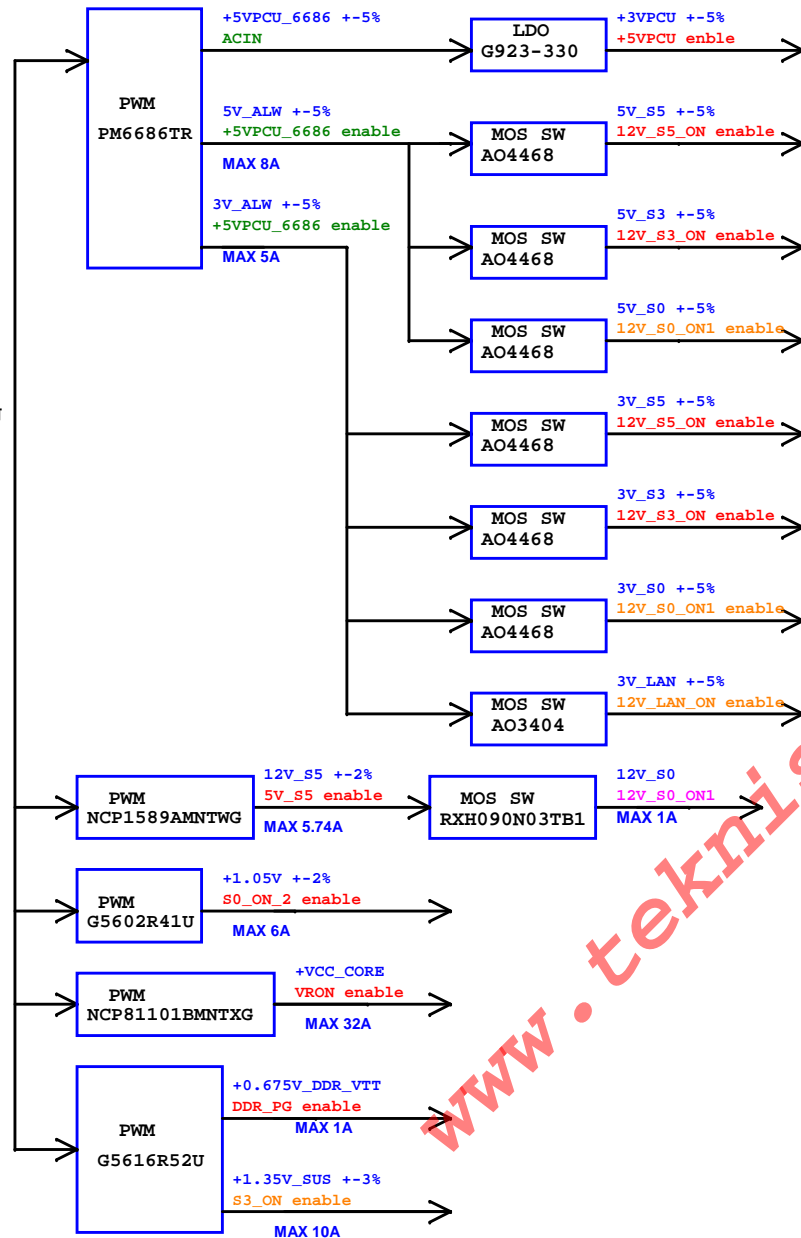
MRT, PR102, PR174, PR111, PR30, PR123, PR127, PR120 change to short pad

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One-Shot 10ms PROCHOT# For ADP

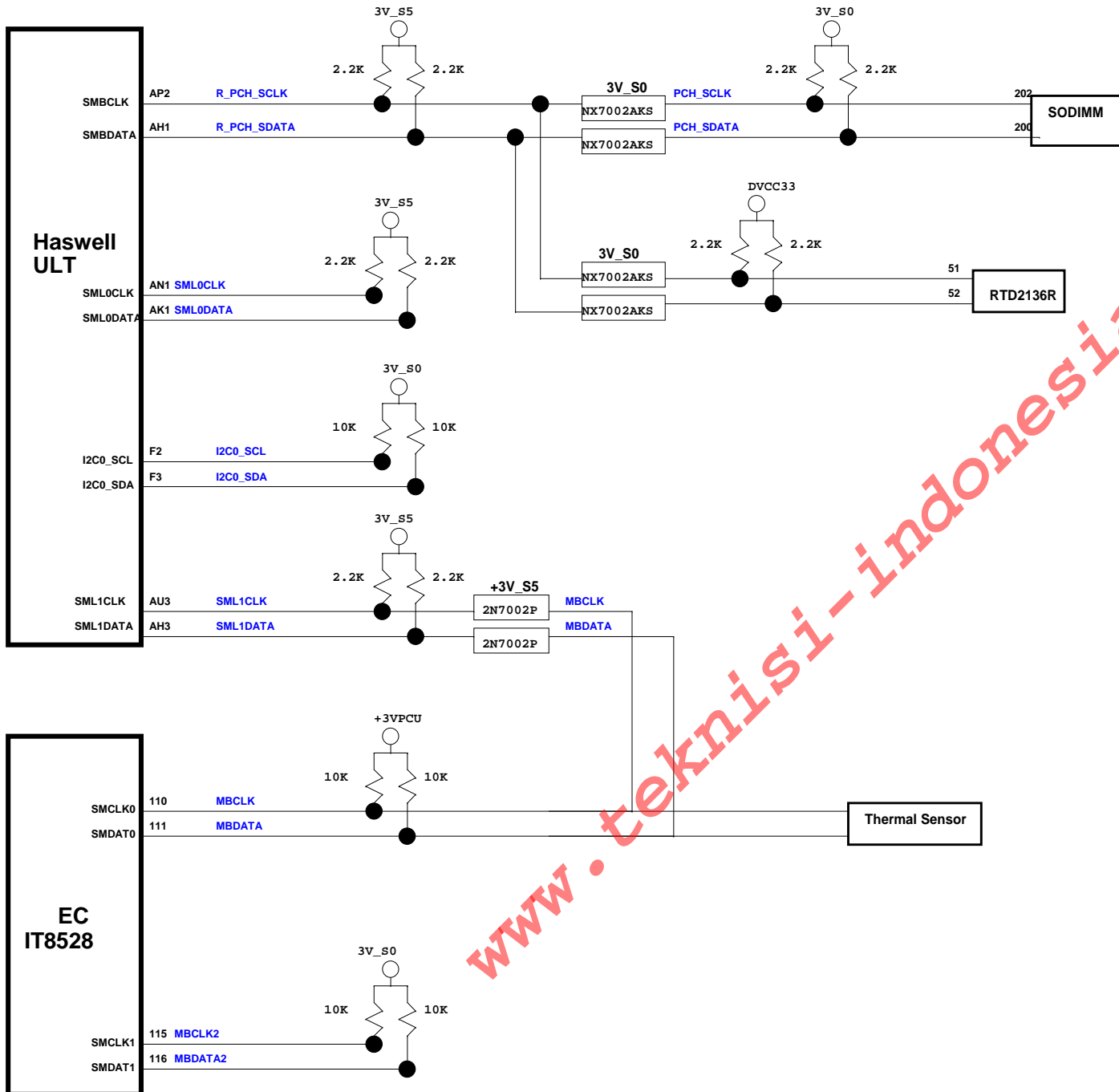






Power Sequence





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Change List

Item	Page	Reason
ES1	All	
ES2	9	Change C66 and C68 to 4.7pf Modify "STAT_ACT#" to PCH
	11	Change C51 and C52 to 10pf
	13	Add off page symbol for "PLTRST#" Add C466 Add C467, Reserved
	18	eDP to LVDS converter change to RTD2136R-CG
	21	AR10 change to 5.1k, AR11 connect to U11.34
	22	AR41,AR42,AR56,AR58,AC40 and AC55 change value
	23	Change Y4 C415 connect to U44 pin 19
	24	Add C468,C469C470 and C471, Reserved
	25	C334 connect to U21 pin 1
	26	Change Y3 Change "ChipResetN" circuit Change C445 and C442 R183 change NU Add C465 R181 change to 0 ohm
	27	Q17 change to DTA124 Add R484
	29	U35 pin 70 change to "HWPG_EC" Add C472, Reserved Change "SATA_ACT#" to PCH "VCCON" change to U35 pin 16 from pin 66 R377 change to NU, R386,R366 change to Stuff
	30	Modify "SATA_ACT#" to PCH SW2 modify pin define Add C473, Reserved
	33	Add PCL121, Reserve
	37	Delete PD16
	39	Add off page symbol of "S3_ON_DIS"
	42	Add net "HWPG_EC" Change power sequence to EC R435,R426,R416,R419,R417,Q26,R414,Q25,R431, C409,R432,U42,C405,R428,C402,R422,U41,C408, R336,C355,C361,U31,R329,R151,C84,U7,C88,C347, U25,R384,R331,U06,C348,R338,R333,C349,U27, C350,U28,C351,R344,C354,U30 change to NU R412,R418,R365,R383,R343,R348 change to Stuff change to meet NEC Recommended Part

Item	Page	Reason
MRT	3	R79 change to short pad
	9	R148 change to short pad
	11	Stuff R102 and R108 and change to 2.2K R261 pin 2 change to "+V1.05S_AXCK_LCPLL" from "+1.05V" Add C486 Nu-stuff RP10 and RP17 chnage to 4.7k ohm
	12	Modify Board ID
	13	R164 change to short pad R494,R495 change to 33 ohm
	14	C59, C60, C304, C306, C275, C276, C290, C291, C54, C55 change to 47uF from 22uF Delete C56, C277, C292, C61, C305 Change L5, L15, L16 R267 change to short pad
	18	R476 connect to R_PCH_SDATA from SML0DATA R475 connect to R_PCH_SCLK from SML0CLK RP18 change to Nu-Stuff RP19 change to 4.7k ohm
	21	AR19, AR31, AR34 change to short pad
	23	R179, R439, R186 change to short pad R437 change to 33 ohm
	24	R501 change to 47 ohm
	26	L24,L25,L26,L27 change to DLP11SN900HL2L from EXC24CG900U R181 change to 33 ohm Remove C123 Stuff R443, Nu-stuff R444 Add R349 100k
	27	L18,L20 change to DLP11SN900HL2L from EXC24CG900U
	29	Stuff R352 and R353 R503 change to 33 ohm
	32	PR73, PR76 change to short pad
	33	Delete PR103, PR104 PR36, PR110, PR112 change to short pad
	34	Delete PR11 PR66, PR8, PR69, PR64, PR4 change to short pad
	35	Delete PR25 PR26, PR93 change to short pad
	37	PF7 change to 6A Stuff P06, PC55
	40	PR102, PR174, PR111, PR30, PR123, PR127, PR120 change to short pad

Item	Page	Reason
PP	3	C33,C32,C30,C28,C35,C34,C31,C29 and R25 change to Nu-Stuff
	9	R37, R30, R38, R39, R33, R36 and R40 change to Nu-Stuff C66 and C68 change to 4pF
	11	Change C51 and C52 to 12pF R102 and R108 chnage to Nu-Stuff
	13	Add U56, R494, R495, R496, R487, R488, R489, R497 Add C481, C482, C477, C478, C483 Nu-Stuff R164, R84 and R504 Stuff E1, R155 and C93 change to Nu-stuff
	17	Remove All HDMI components R229, R225, R231, R227, R221, R205, R217, R218, L14, C153, C154, C157, C152, C151, C167, C168, C169, R219, U18, R201, R206, R215, R223, D12, R197, R6, F11, R9, R8, R7, D1, L2, C6, CN3, D11
	18	R471 change to 2.2K
	19	R170 change to NU
	22	AU7 changed to TPA4411MRTJ from MAX4411 AR43, AR44 change to 5.6K from 6.2K AR58 change to 1.78K from 2K AR56 change to 15K from 16K AR42 change to 16K from 15K
	23	Change C423 and C424 to 10pF AC28 and AC29 change to size 0805, 25V
	24	Add R485, R486, R490, R491, R492, R493, R498, R499, R500 and R501 Nu-stuff C484, C485, C468, C469, C470, C471, C474, C475, C478 and C480
	25	Stuff C300, C299,C333,C332 and add C476 reserved U21 pin 1 change to "PLTRST#_1" from "BUF_PLT_RST#"
	26	Stuff R187 Change C129 and C133 to 12 pF
	27	Stuff R335 Add Q35, Q39, R512 and Q17 change to Nu-stuff U32 change to MAX14603 from MAX14641
	28	C5 change to 22pF
	29	U35 pin 22 chnage to "BUF_PLT_RST#" from "PLTRST#" "EC_APWROK_R" change to pin 85 from pin 106 Add R503, R513, R514, R515, Q36, Q37, Q38, Q40, Q41, Q42 Q20, Q23, Q24, SW3, R392, R352, R353, R153, C87, R159, R156, LED3, LED4 chngne to Nu-stuff
	30	U19 pin 16 chnage to "PLTRST#_1" from "PLTRST#" Q2 change to IRLML9303TRPBF from AO3409
	31	F3 change to 3A from 1A
	37	Discharge circuit change to VIN from VA+